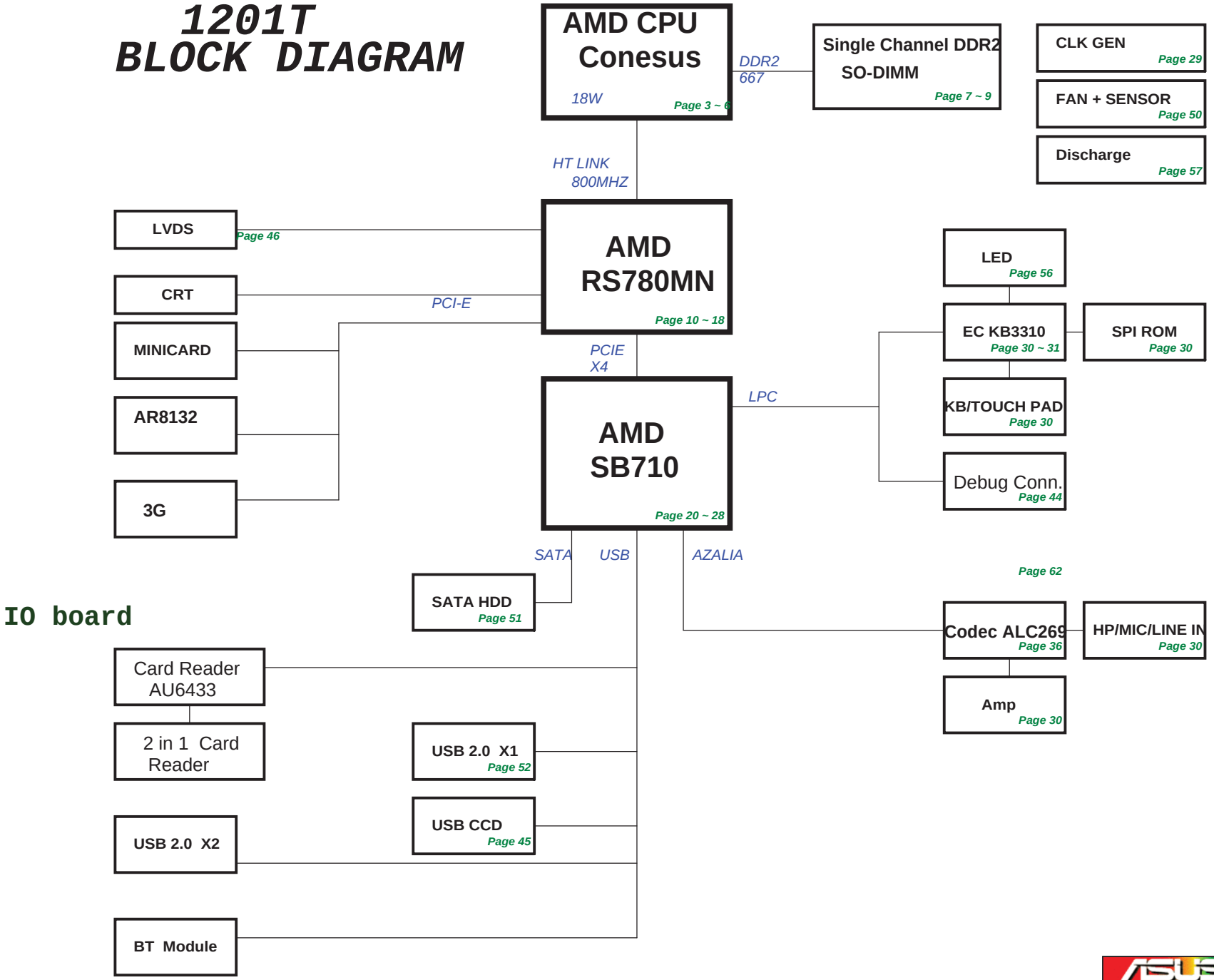
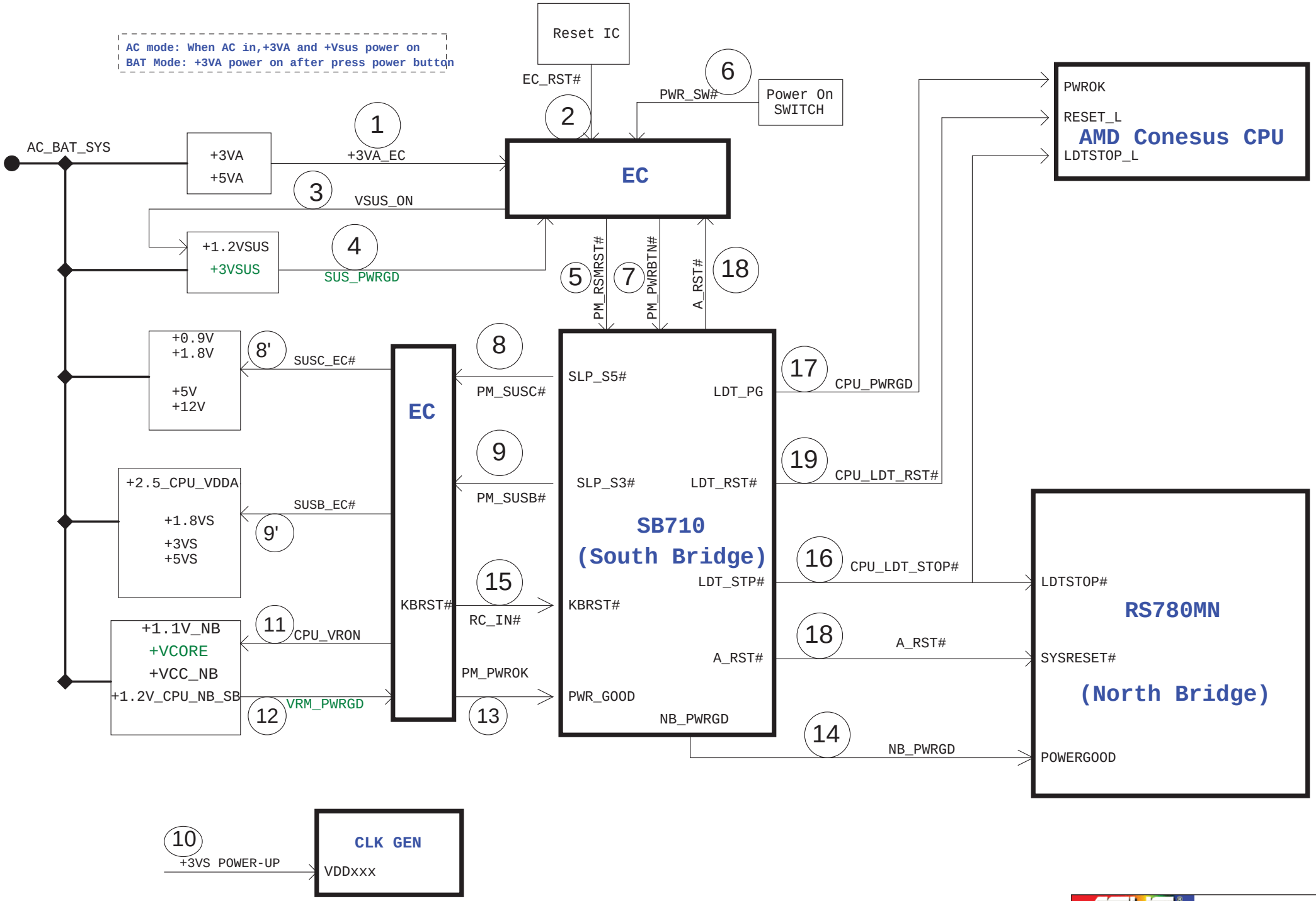
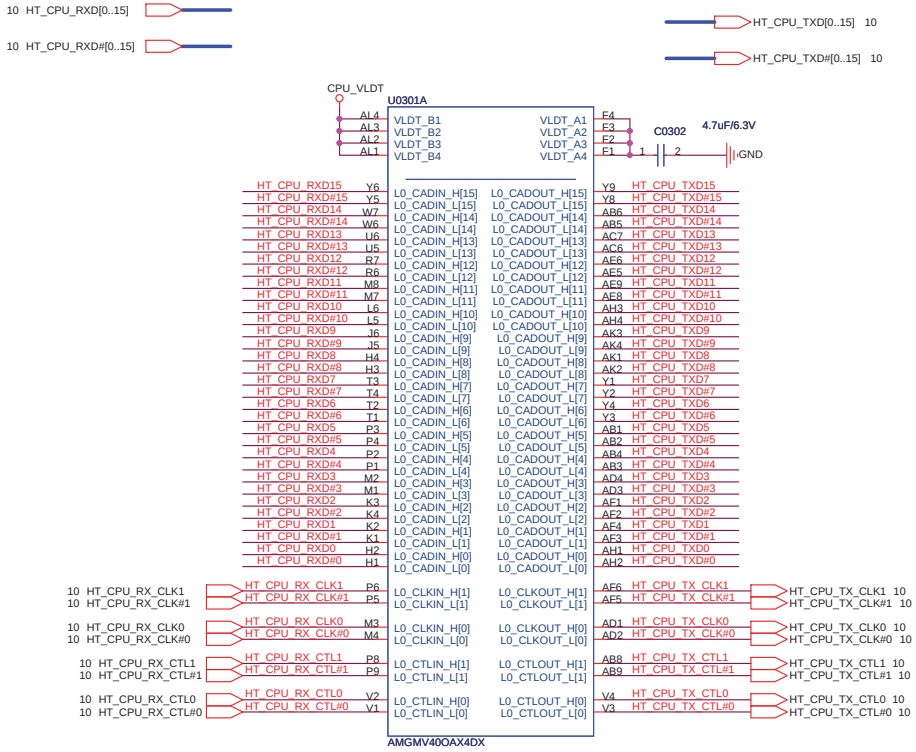
1201T BLOCK DIAGRAM



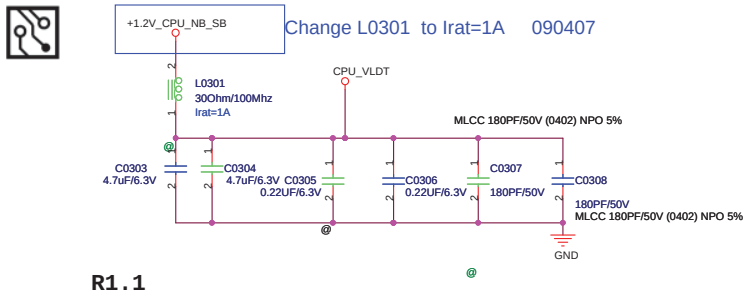
ASUSTeK Computer INC	Title : Block Diagram	
	Engineer: N/A	
Size: Custom	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 1 of 79	



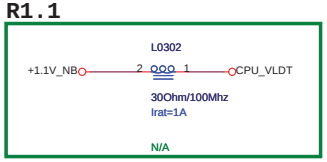
ASUSTeK.Computer.INC	Title : Power sequence		
	Engineer: N/A		
Size: Custom	Project Name: 1201T		Rev: 2.0
Date: Wednesday, October 21, 2009	Sheet 2 of 79		



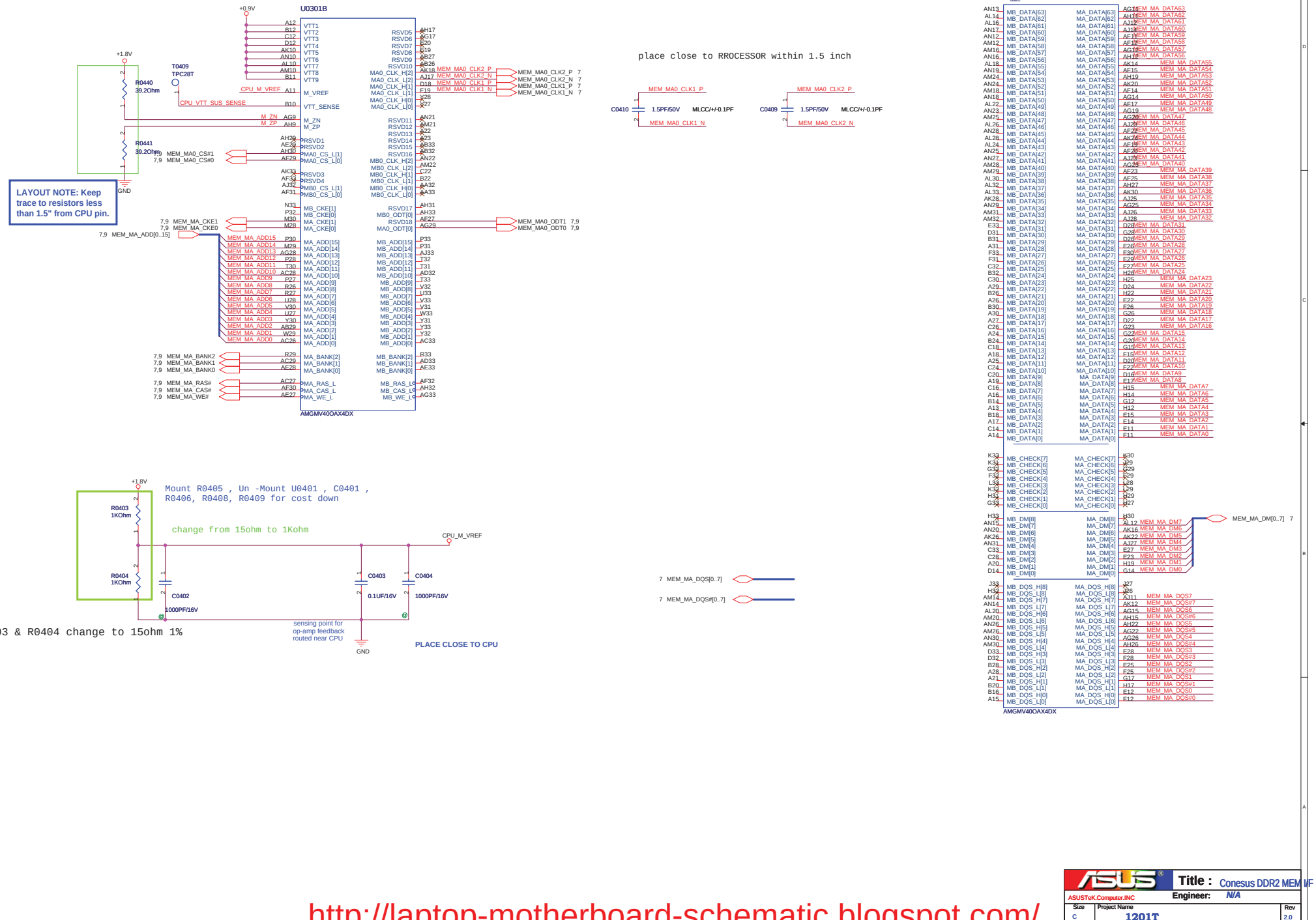
DESIGN NOTE:
VLDT must be routed as a pour or a trace at least 200 mils wide.
VLDT may be routed from the source to either ALx balls or Fx balls.
Choose whichever makes routing simpler.
These six capacitors must be placed very near the selected balls.
The "other" set of balls must be decoupled with a 4.7uF cap.



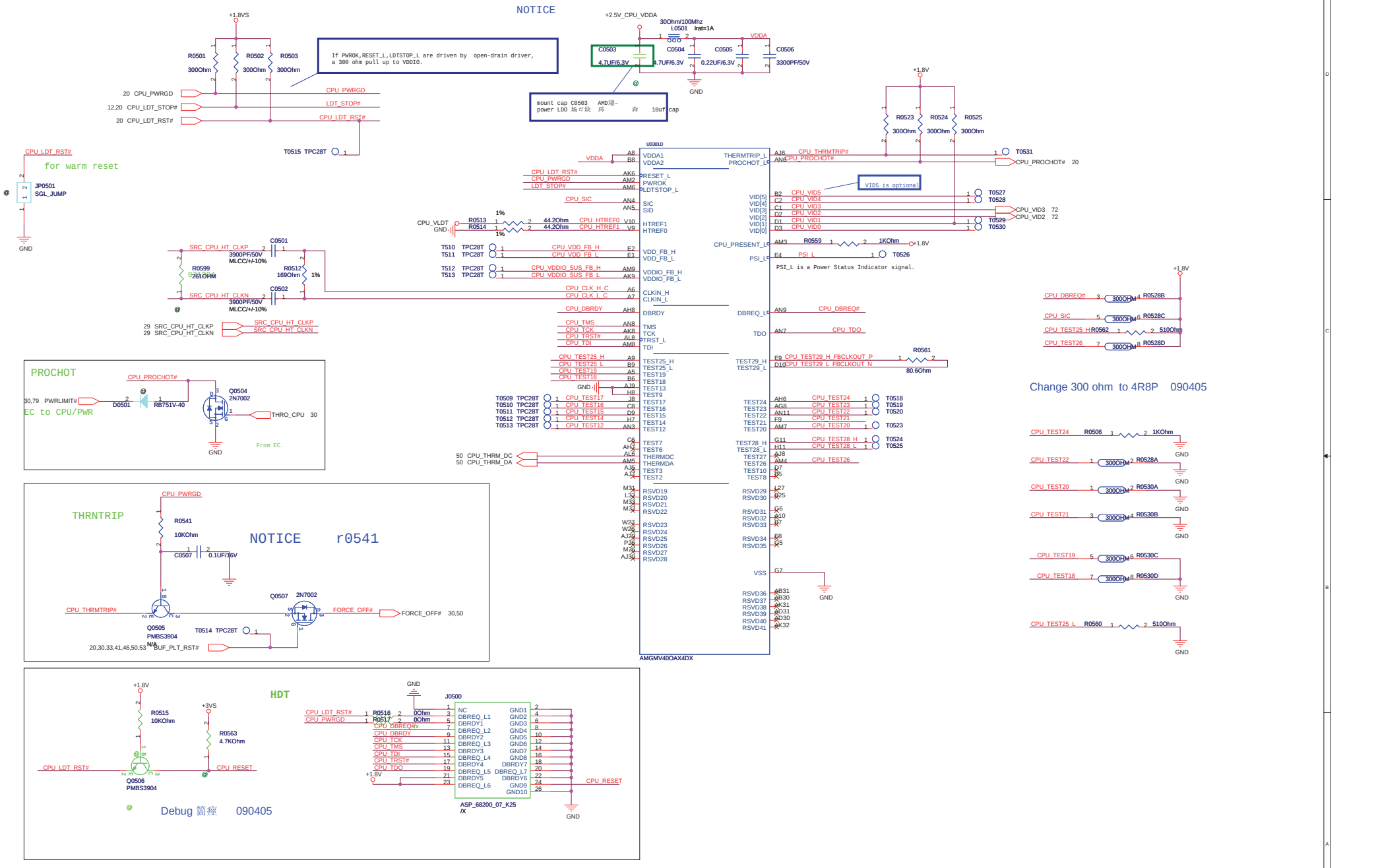
R1.1



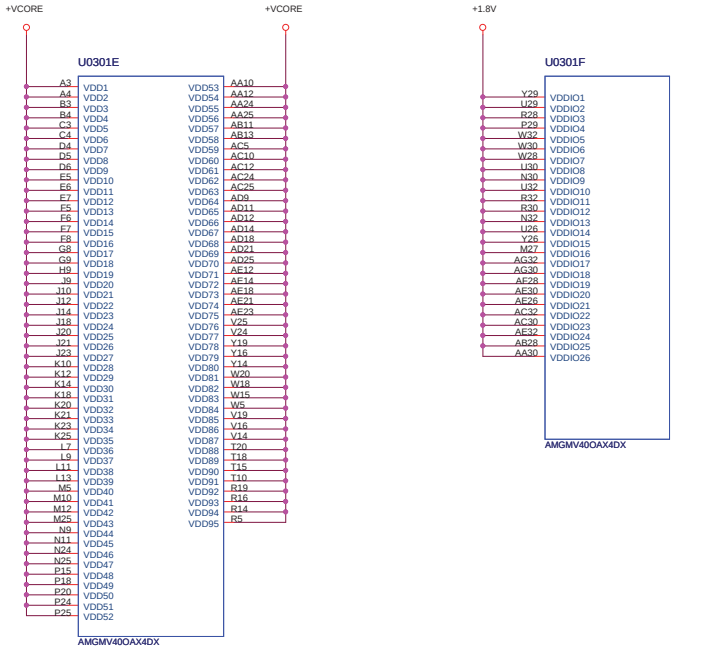
ASUSTeK.Computer.INC	Title : Conesus HT I/F	
	Engineer: N/A	
Size: Custom	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 3 of 79	

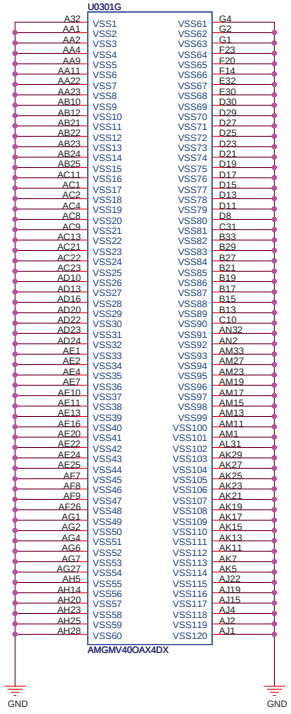


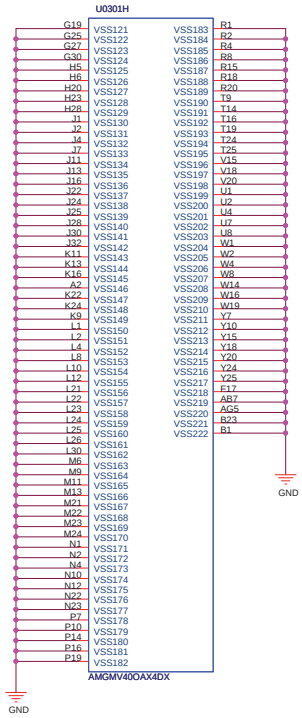
ASUSTeK.Computer.INC	Title : Conesus DDR2 MEM I/F	
	Engineer: N/A	
Size: C	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 4 of 79	

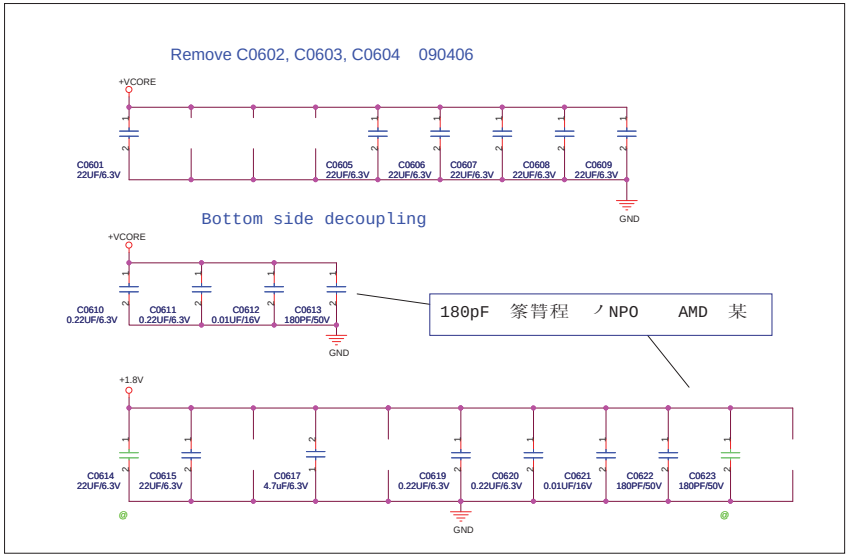


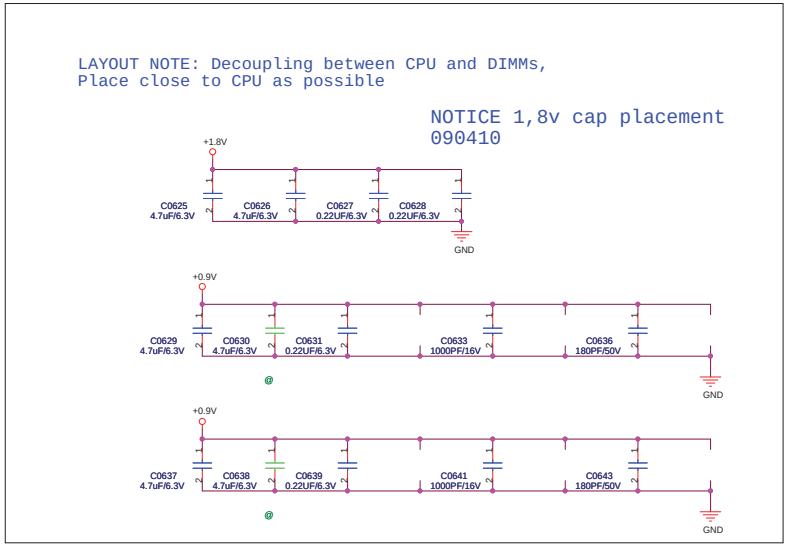
ASUSTeK.Computer.INC	Title Gonesus CNT/DBG/THERM	
	Engineer: N/A	
Size C	Project Name 1201T	Rev 2.0
Date: Wednesday, October 14, 2009	Sheet 5 of 79	











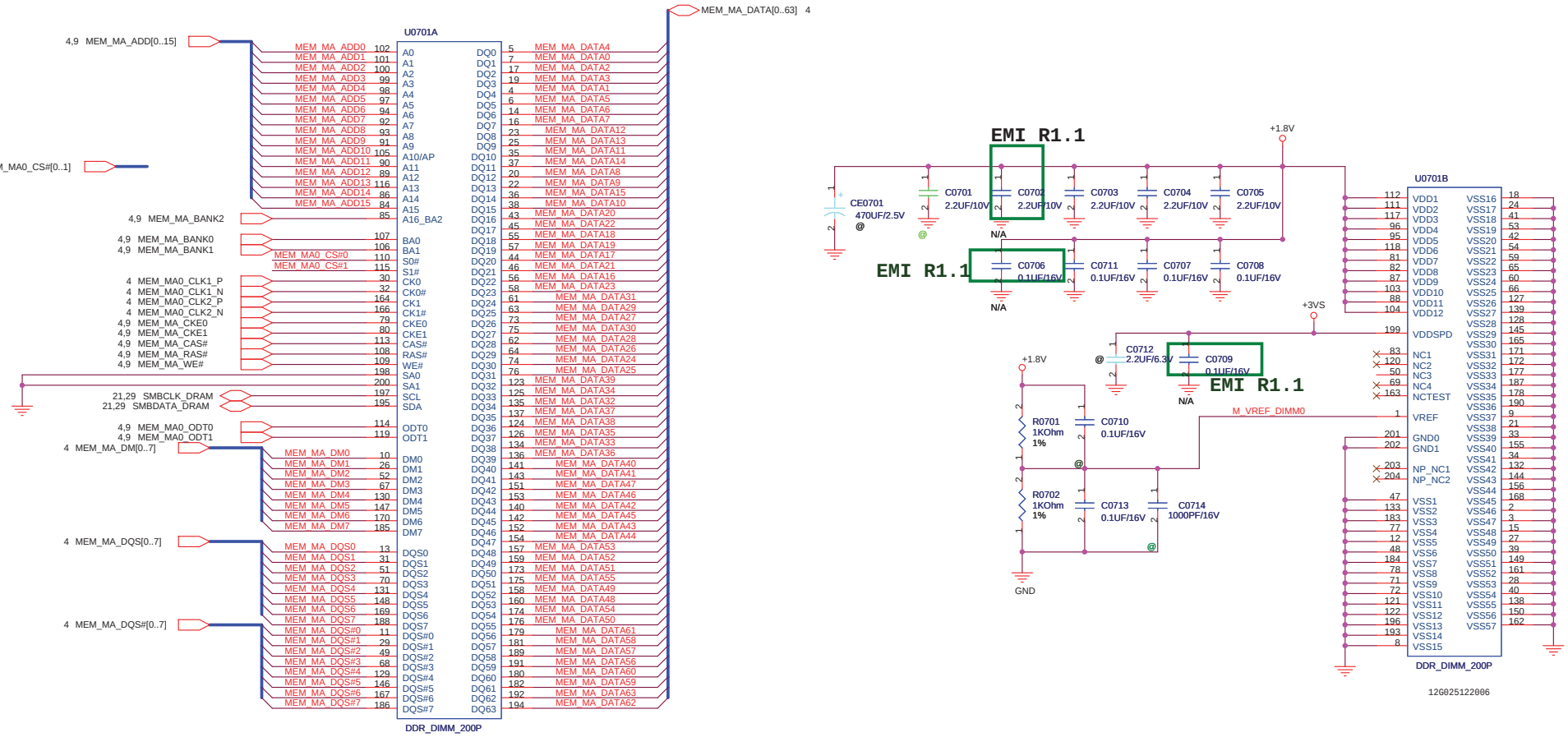
ASUSTeK.COMPUTER.INC

Title : Conesus Power

Engineer: N/A

Size	Project Name	Rev
C	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 6 of 79



12G02533200D

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM0

Engineer:

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 7 of 79

4,7 MEM_MA_ADD[0..15]

4,7 MEM_MA_BANK2 — MEM_MA_BANK2
4,7 MEM_MA_BANK1 — MEM_MA_BANK1
4,7 MEM_MA_BANK0 — MEM_MA_BANK0

4,7 MEM_MA0_ODT0 — MEM_MA0_ODT0
4,7 MEM_MA0_ODT1 — MEM_MA0_ODT1

4,7 MEM_MA_CKE0 — MEM_MA_CKE0
4,7 MEM_MA_CKE1 — MEM_MA_CKE1

4,7 MEM_MA_RAS# — MEM_MA_RAS#
4,7 MEM_MA_CAS# — MEM_MA_CAS#
4,7 MEM_MA_WE# — MEM_MA_WE#

4,7 MEM_MA0_CS#0 — MEM_MA0_CS#0
4,7 MEM_MA0_CS#1 — MEM_MA0_CS#1

change to 8R16P 090405

+0.9V

47OHM

MEM_MA_ADD10	8	47OHM	9	RN0901H	C0901	0.1UF/16V
MEM_MA_ADD0	7	47OHM	10	RN0901G		
MEM_MA_RAS#	6	47OHM	11	RN0901F		
MEM_MA_ADD14	6	47OHM	11	RN0903F		
MEM_MA_ADD5	8	47OHM	9	RN0905H	C0902	0.1UF/16V
MEM_MA_WE#	4	47OHM	13	RN0905D		
MEM_MA_ADD1	6	47OHM	11	RN0905F		
MEM_MA_ADD11	3	47OHM	14	RN0903C		
MEM_MA_ADD7	4	47OHM	13	RN0903D	C0903	0.1UF/16V
MEM_MA_CKE0	7	47OHM	10	RN0903G		
MEM_MA_ADD6	1	47OHM	16	RN0903A		
MEM_MA_ADD2	4	47OHM	13	RN0901D		
MEM_MA_ADD15	5	47OHM	12	RN0903E	C0912	0.1UF/16V
MEM_MA_CKE1	8	47OHM	9	RN0903H		
MEM_MA_ADD4	2	47OHM	15	RN0903B		
MEM_MA_ADD3	7	47OHM	10	RN0905G		
MEM_MA_BANK0	5	47OHM	12	RN0905E	C0913	0.1UF/16V
MEM_MA0_CS#0	2	47OHM	15	RN0901B		
MEM_MA_CAS#	3	47OHM	14	RN0905C		
MEM_MA0_ODT1	1	47OHM	16	RN0905A	C0914	0.1UF/16V
MEM_MA0_CS#1	2	47OHM	15	RN0905B		
MEM_MA0_ODT0	3	47OHM	14	RN0901C		
MEM_MA_ADD13	1	47OHM	16	RN0901A	C0915	0.1UF/16V
MEM_MA_BANK1	5	47OHM	12	RN0901E		
MEM_MA_ADD12	5	47Ohm	6	RN0909C		
MEM_MA_BANK2	7	47Ohm	8	RN0909D		
MEM_MA_ADD8	1	47Ohm	2	RN0909A	C0916	0.1UF/16V
MEM_MA_ADD9	3	47Ohm	4	RN0909B		

All outputs: +1.8V

Remove1.8V C0910,C0911 0.1uF 090405

+0.9V

0.1UF/16V	C0904	0.1UF/16V	C0905	0.1UF/16V	C0906
0.1UF/16V	C0907	0.1UF/16V	C0908	0.1UF/16V	C0909

GND

EMI R1.1

+1.8V

0.1UF/16V	C0933	0.1UF/16V	C0934	0.1UF/16V	C0935	0.1UF/16V	C0936	0.1UF/16V	C0937	0.1UF/16V	C0938
@		@		N/A		N/A		N/A		N/A	

GND

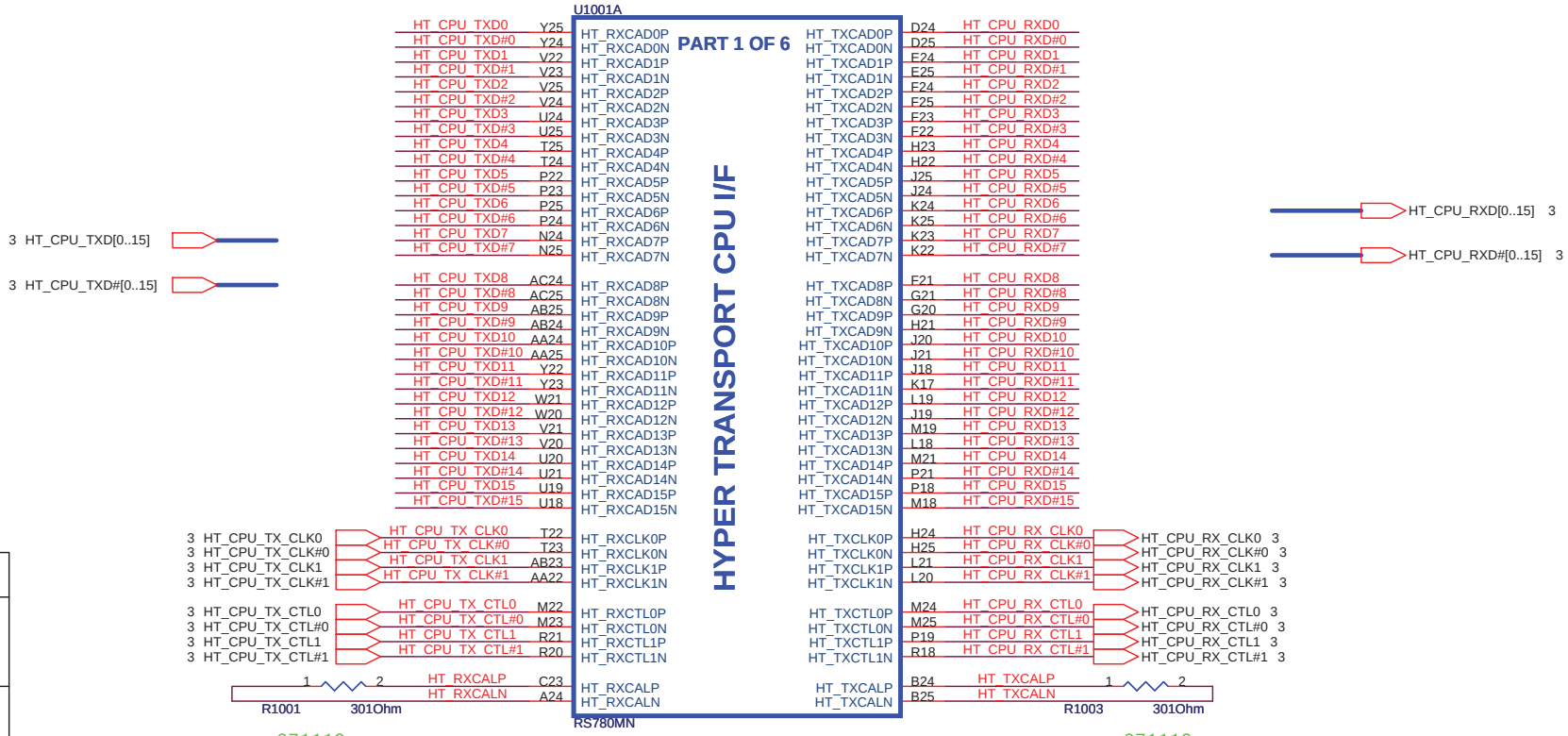
PLACE CLOSE TO SOCKET(PER EMI/EMC)

090818 Swap for Layout

ASUSTeK COMPUTER INC	Title : DDR2_TERMINATIONS	
	Engineer:	
Size: Custom	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 9 of 79	

R1.11 080319

Change the NB Part number to RS780 (A13)



Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

071119
change R1001 value

071119
change R1003 value

ASUSTeK.Computer.INC

Title : RS780M-HT LINK I/F

Engineer: N/A

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 10 of 79

R1.11 080319

Change the NB Part number to RS780 (A13)

PCIE 0	WLAN
PCIE 1	GLAN
PCIE 2	3G

Add Test Point

T1106 TPC28T, T1105 TPC28T, T1104 TPC28T, T1103 TPC28T, T1107 TPC28T, T1108 TPC28T

U1001B

PART 2 OF 6

PCIE I/F GFX

GFX_RX0P D4, GFX_RX0N C4, GFX_RX1P A3, GFX_RX1N B3, GFX_RX2P C2, GFX_RX2N C1, GFX_RX3P E5, GFX_RX3N F5, GFX_RX4P G5, GFX_RX4N G6, GFX_RX5P H5, GFX_RX5N H6, GFX_RX6P J6, GFX_RX6N J5, GFX_RX7P J7, GFX_RX7N J8, GFX_RX8P L5, GFX_RX8N L6, GFX_RX9P M8, GFX_RX9N L8, GFX_RX10P P7, GFX_RX10N M7, GFX_RX11P P5, GFX_RX11N M5, GFX_RX12P R8, GFX_RX12N P8, GFX_RX13P R6, GFX_RX13N R5, GFX_RX14P P4, GFX_RX14N P3, GFX_RX15P T4, GFX_RX15N T3

GFX_TX0P A5, GFX_TX0N B5, GFX_TX1P A4, GFX_TX1N B4, GFX_TX2P C3, GFX_TX2N B2, GFX_TX3P D1, GFX_TX3N D2, GFX_TX4P E2, GFX_TX4N E1, GFX_TX5P F4, GFX_TX5N E3, GFX_TX6P F1, GFX_TX6N E2, GFX_TX7P H4, GFX_TX7N H3, GFX_TX8P H1, GFX_TX8N H2, GFX_TX9P J2, GFX_TX9N J1, GFX_TX10P K4, GFX_TX10N K3, GFX_TX11P K1, GFX_TX11N K2, GFX_TX12P M4, GFX_TX12N M3, GFX_TX13P M1, GFX_TX13N M2, GFX_TX14P N2, GFX_TX14N N1, GFX_TX15P P1, GFX_TX15N P2

PCIE I/F GPP

GPP_RX0P AE3, GPP_RX0N AD4, GPP_RX1P AE2, GPP_RX1N AD3, GPP_RX2P AD1, GPP_RX2N AD2, GPP_RX3P V5, GPP_RX3N W6, GPP_RX4P U5, GPP_RX4N U6, GPP_RX5P U8, GPP_RX5N U7

GPP_TX0P AC1, GPP_TX0N AC2, GPP_TX1P AB4, GPP_TX1N AB3, GPP_TX2P AA2, GPP_TX2N AA1, GPP_TX3P Y1, GPP_TX3N Y2, GPP_TX4P Y4, GPP_TX4N Y3, GPP_TX5P V1, GPP_TX5N V2

PCIE I/F SB

SB_RX0P AA8, SB_RX0N Y8, SB_RX1P AA7, SB_RX1N Y7, SB_RX2P AA5, SB_RX2N AA6, SB_RX3P W5, SB_RX3N Y5

SB_TX0P AD7, SB_TX0N AE7, SB_TX1P AE6, SB_TX1N AD6, SB_TX2P AB6, SB_TX2N AC6, SB_TX3P AD5, SB_TX3N AE5

PCE_CALRP AC8, PCE_CALRN AB8

RS780MN

53 PCIE_RXP0_MINICARD, 53 PCIE_RXN0_MINICARD, 33 PCIE_RXP1_LAN, 33 PCIE_RXN1_LAN, 41 PCIE_RXP2_3G, 41 PCIE_RXN2_3G

GPP_TX0P_C C1101 2 1 0.1UF/10V, GPP_TX0N_C C1103 2 1 0.1UF/10V, GPP_TX1P_C C1102 2 1 0.1UF/10V, GPP_TX1N_C C1105 2 1 0.1UF/10V, GPP_TX2P_C C1104 2 1 0.1UF/10V, GPP_TX2N_C C1106 2 1 0.1UF/10V

/3.5G Add 3G /3.5G

PCIE_TXP0_MINICARD 53, PCIE_TXN0_MINICARD 53, PCIE_TXP1_LAN 33, PCIE_TXN1_LAN 33, PCIE_TXP2_3G 41, PCIE_TXN2_3G 41

20 PCIE_SB_NB_RX0P, 20 PCIE_SB_NB_RX0N, 20 PCIE_SB_NB_RX1P, 20 PCIE_SB_NB_RX1N, 20 PCIE_SB_NB_RX2P, 20 PCIE_SB_NB_RX2N, 20 PCIE_SB_NB_RX3P, 20 PCIE_SB_NB_RX3N

A_TX0P_C C1107 2 1 0.1UF/10V, A_TX0N_C C1109 2 1 0.1UF/10V, A_TX1P_C C1108 2 1 0.1UF/10V, A_TX1N_C C1111 2 1 0.1UF/10V, A_TX2P_C C1110 2 1 0.1UF/10V, A_TX2N_C C1113 2 1 0.1UF/10V, A_TX3P_C C1112 2 1 0.1UF/10V, A_TX3N_C C1114 2 1 0.1UF/10V

PCIE_NB_SB_TX0P 20, PCIE_NB_SB_TX0N 20, PCIE_NB_SB_TX1P 20, PCIE_NB_SB_TX1N 20, PCIE_NB_SB_TX2P 20, PCIE_NB_SB_TX2N 20, PCIE_NB_SB_TX3P 20, PCIE_NB_SB_TX3N 20

PCE_CALRP, PCE_CALRN

1.27KOhm 1 2 R1101, 2KOHM 1 2 R1102, +1.1V_NB

GND

071129

Add net name

071212

change P/N

ASUSTeK.Computer.INC

Title : RS780M-PCIE LINK I/F

Engineer: N/A

Size	Project Name	Rev
Custom	12O1T	2.0

Date: Wednesday, October 14, 2009 Sheet 11 of 79

notice L1201 L1204 change SL?
090411

09.7.14

080201 R1.1
Change to +1.1V_NB
form NB_VDD_MUX

R1.11
080310

090407

R2.0080401
Change NB_ALLOW_LDTSTOP to ALLOW_LDTSTOP

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

R1.11
080319
Change the NB Part number to RS780 (A13)

remove D1201 circuit
090410

080325
R2.0 Remove Q1201A and R1219

071218
for measurement near U1001

071204
DEL serial R

?? for external graphic

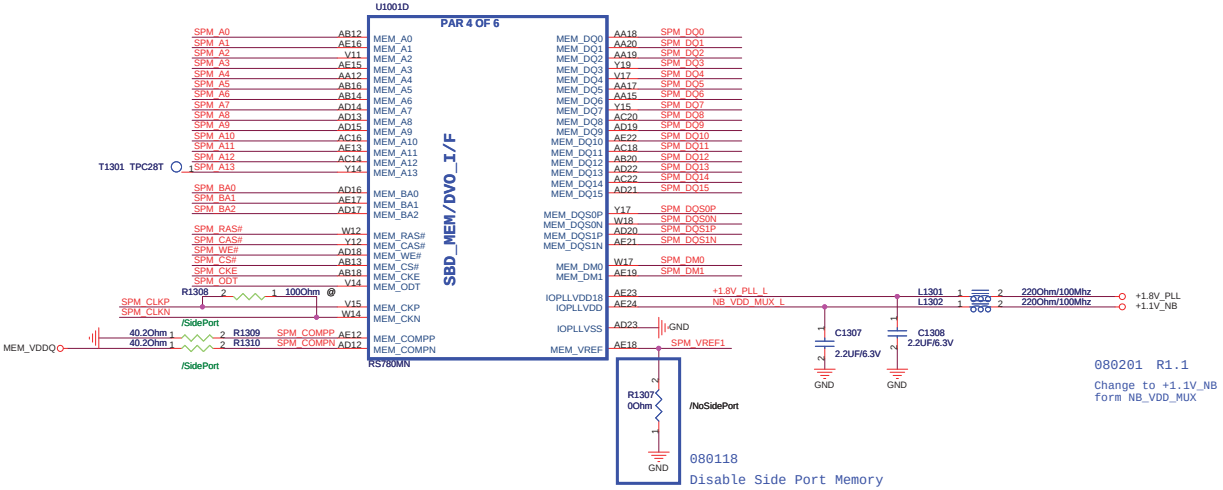
have via for measurement

R2.0080401
Change NB_ALLOW_LDTSTOP to ALLOW_LDTSTOP

ASUSTeK.COMPUTER.INC	Title : RS780M-SYS I/F	
	Engineer: N/A	
Size: C	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 12 of 79	

R1.11 080319

Change the NB Part number to RS780 (A13)



080201 R1.1

Change to +1.1V_NB form NB_VDD_MUX

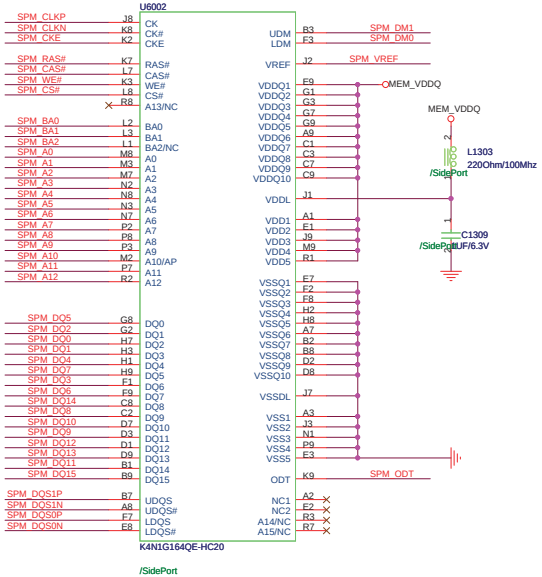
080118

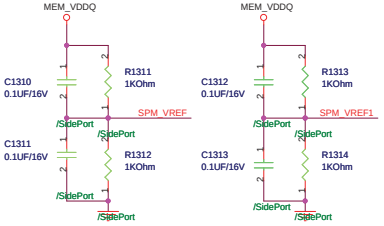
Disable Side Port Memory

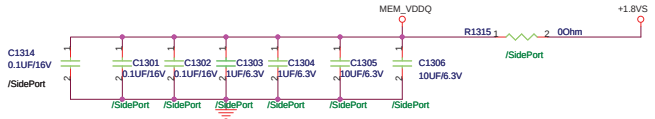
R1.1

090813

Reserve Side Port Memory







DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

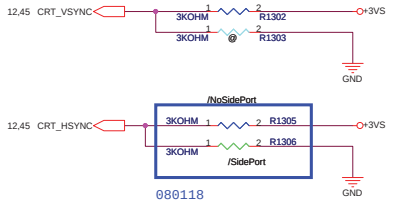
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



080118

Disable Side Port Memory

R1.1

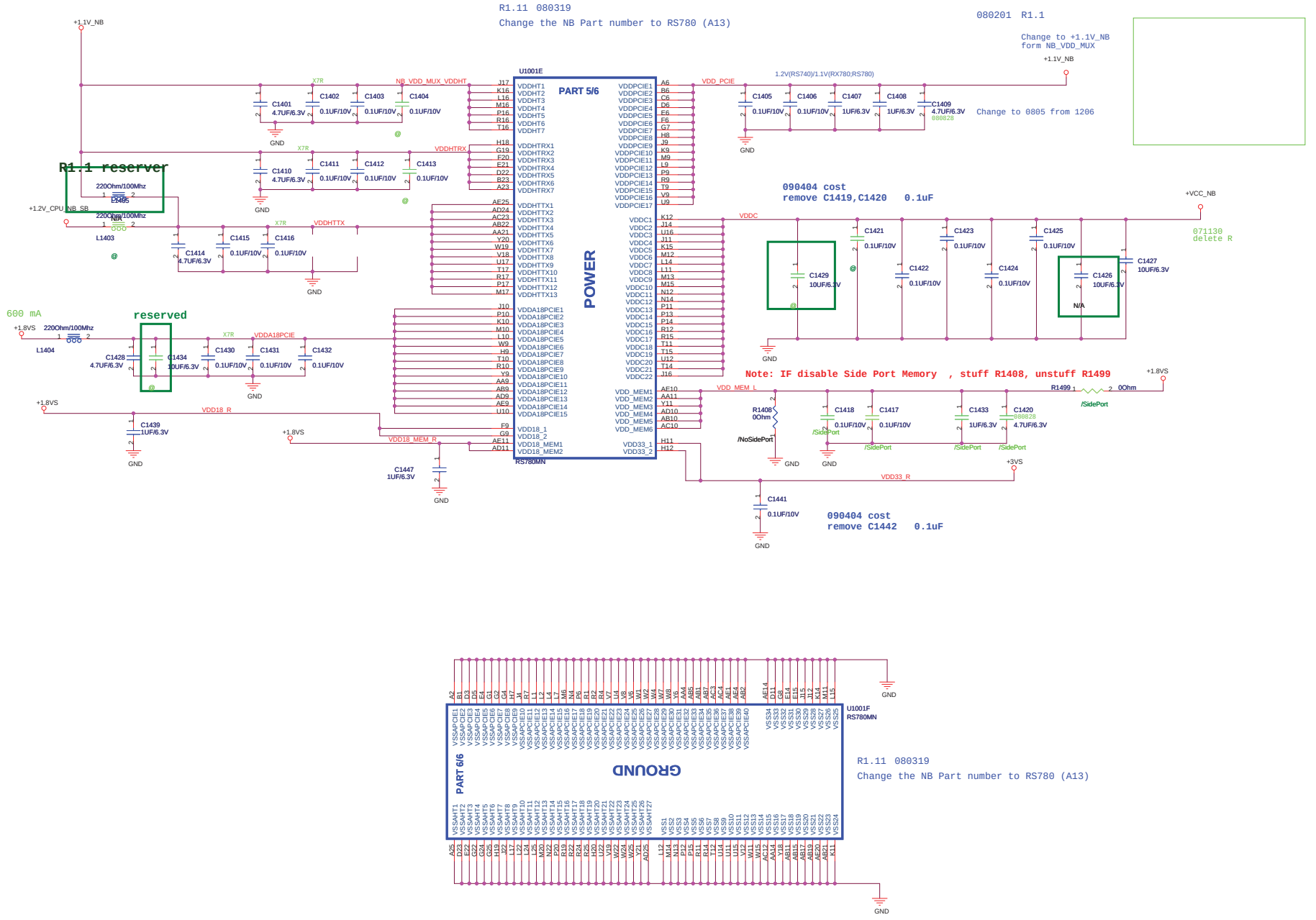
ASUSTeK.Computer.INC

Title : RS780M-SPMEM/STRAP

Engineer: N/A

Size	Project Name	Rev
C	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 13 of 79



ASUSTeK.COMPUTER.INC	Title : RS780M-POWER	
	Engineer: N/A	
Size: C	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 14 of 79	

R2.0 080327
Add test point for factory
ICT test

R1.11 080319
Change the SB Part number to SB700 (A12)

071120
add net name

071204
AMD review

EC LPC CLK

SB700
Part 1 of 5

071207
AMD
review

Del T2052~T2074 for
GND Via improvement

080218 R1.1
Add Test Point

Reserved Via

080218 R1.1
Add Test Point

internal Pull Up 15K

internal Pull Up 8.2K

071212
change P/N

090403

071121

Correct to R1.1

071218
for measurement
near U2001
del R2007,R2011

080212
R1.1
Del T2017~T2033 for
GND Via improvement

Add net SB_OSC
090326

EMI
090414

R2.0 080327

change C2015,C2016 to 22pF 090407

暗BOM 璩 传ΘSB710 腹:02G050003001
090406

change ctystal (SB710) 07G010413277
090331

S_BATT

ASUSTeK.COMPUTER.INC	Title : SB700_CPU/PCIE/LPC/CLK	
	Engineer: N/A	
Size: C	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 20 of 79	

R1.11 080319
Change the SB Part number to SB700 (A12)

071129
Add net name

SB700 Part 4 of 5

U2001D

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3 /GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3 /GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB MISC

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N

USB 1.1

USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USB 2.0

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

USBCLK_48_SB
R2104 8.87KOhm
USBCLK_48 29
GND

R1.1

USB_PP12 27
USB_PN12 27
Bluetooth

USB_PP8 35
USB_PN8 35
CCD

USB_PP4 28
USB_PN4 28
AU6433

USB_PP3 41
USB_PN3 41
3G

USB_PP2 28
USB_PN2 28
IO board USB Connector

USB_PP1 28
USB_PN1 28
IO board USB Connector

USB_PP0 52
USB_PN0 52
USB CONN

SB_GP16 24
SB_GP17 24
for strap

071120 T2122 T2124 TPC28T TPC28T

071119
30 EXT_SMI#
30 EXT_SCI#
30 PM_SUSB#
30 PM_SUSC#
30 PM_PWRBTN#
32 PM_PWROK
12 SUS_STAT#
T2101 TPC28T

071119
30 A20GATE
30 RC_IN#
071204
TEST2
TEST1
TEST0

071207
RS780 POWERGOOD
is 1.8VS rail
+1.8VS
R2137 300OHm
(I / PU)
T2105 TPC28T
T2107 TPC28T
T2117 TPC28T
SYS_REST#
33,53 PCIE_WAKE#
SB_THRMTRIP#
T2106 TPC28T
T2108 TPC28T
NB_PWRGD_R
12 NB_PWRGD

32 PM_RSMRST#

T2121 TPC28T

T2118 TPC28T
T2102 TPC28T
071127
GPIO10
GPIO6
PCB_ID1
GPIO0
GPIO39
GPIO40
SB_SPKR_R

T2109 TPC28T
T2103 TPC28T
T2110 TPC28T

7,29 SMBCLK_DRAM
7,29 SMBDATA_DRAM
09.7.13

T2126 TPC28T
071204
T2123 TPC28T
T2113 TPC28T

T2111 TPC28T
T2104 TPC28T
GPIO8
GPIO66 071127
PCB_ID2
DDR3_RST# Via

T2112 TPC28T
080118 Reserve Via

T2114 TPC28T
T2116 TPC28T
28 USB_OC#2
52 USB_OC#0

ACZ_BCLK
ACZ_SDOUT
28 ACZ_SDIN0_AUD

080212
Del T2115 and T2116 for GND Via
improvement (GPIO44 and 46)

ACZ_SYNC
ACZ_RST#
GPM8# VIA
T2115 TPC28T
080218 R1.1
Add Test Point

internal P/U 8.2k
22 PCB_ID0
PCB_ID2
PCB_ID1
PCB_ID0
R2117 4.7KOhm
R2118 4.7KOhm
R2119 4.7KOhm

T2119 TPC28T
T2120 TPC28T
SPI_CS2#

071203
SUS_STAT# R2110 4.7KOhm
AMD review
GND

071119
S0 power
+3VS
SUS_STAT# R2109 4.7KOhm
SMBCLK_DRAM
SMBDATA_DRAM
2.2KOHM RN2112D
2.2KOHM RN2112C

090404 cost

09.7.13
+3VSUS
2.2KOHM RN2112A
2.2KOHM RN2112B

TEST2 R2120 2.2kOHM
TEST1 R2121 2.2kOHM
TEST0 R2132 2.2kOHM
071204 AMD review

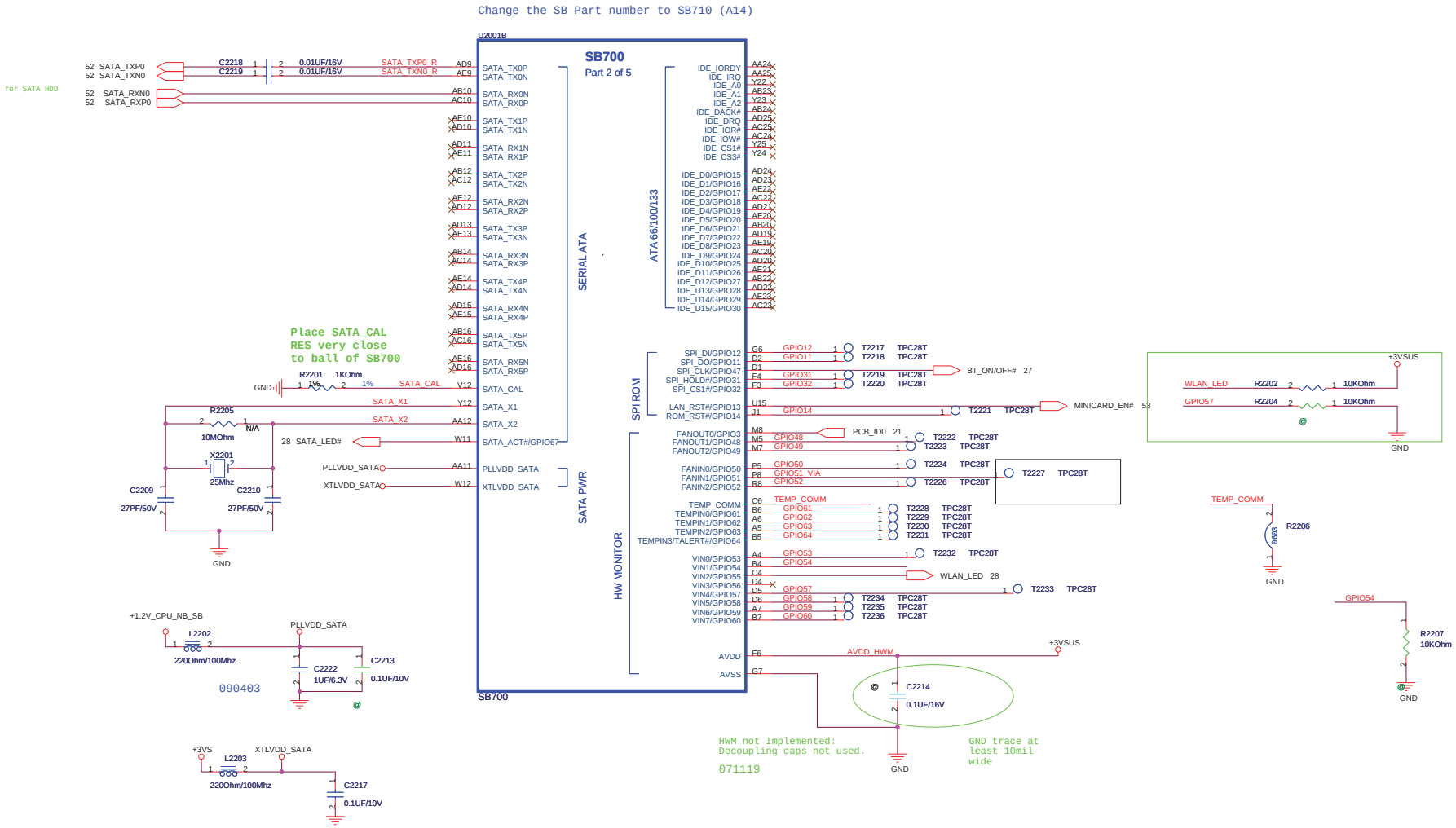
+3VSUS
EXT_SMI# R2135 10KOhm
EXT_SCI# R2136 10KOhm

071204
AMD review
ACZ_SDIN0_AUD R2134 10KOhm

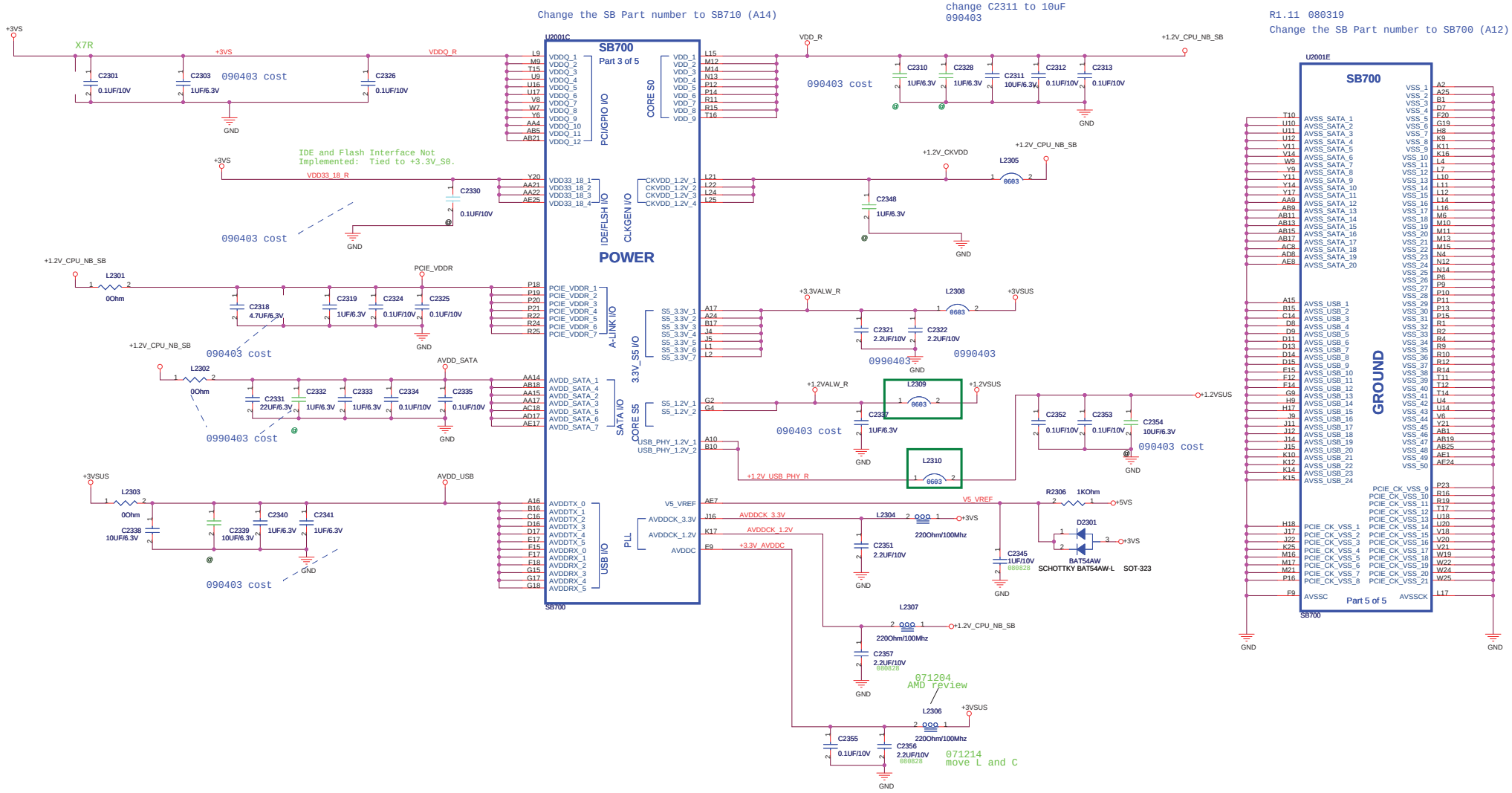
PUT AT SB700 SIDE
Change 33ohm to 4R8P 090405
for strap
24 ACZ_RST#
ACZ_RST# 33OHM R2123A ACZ_RST#_AUD
ACZ_RST#_AUD 28
SB700A11 EC enable Strap Workaround
EMI 090415
C2148 22PF/50V /EMI
ACZ_BCLK 33OHM R2123D ACZ_BCLK_AUD
ACZ_BCLK_AUD 28
@ R2133 10KOhm
AMD review
ACZ_SYNC 33OHM R2123B ACZ_SYNC_AUD
ACZ_SYNC_AUD 28
ACZ_SDOUT 33OHM R2123C ACZ_SDOUT_AUD
ACZ_SDOUT_AUD 28

need to modify topology??

ASUSTeK.COMPUTER.INC
Title : SB700_GPIO/USB/HD/ACPI
Engineer: N/A
Size C
Project Name 1201T
Rev 2.0
Date: Wednesday, October 14, 2009
Sheet 21 of 79



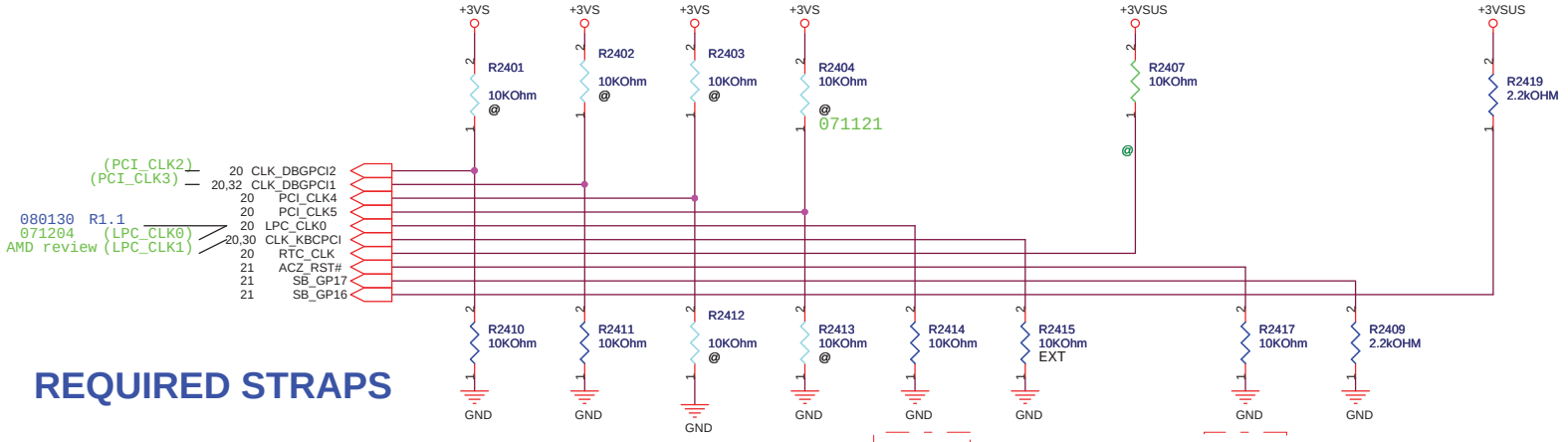
Title :	SB700_PATA/SATA
ASUSTeK.Computer.INC	Engineer: N/A
Size: Custom	Project Name: 1201T
Rev: 2.0	
Date: Wednesday, October 14, 2009	Sheet 22 of 79



Title : SB700_POWER		
ASUSTeK.Computer.INC	Engineer: N/A	
Size: C	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 23 of 79	

Remove R2405, R2406,R2416
R2408, R2418, R2420, R2418 090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

For SB700 A12 and later version

080204 R1.1
Change the Text Comment

ASUSTeK.Computer.INC	Title : SB700_STRAP		
	Engineer: N/A		
Size: Custom	Project Name: 1201T		Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 24 of 79		

<Variant Name>

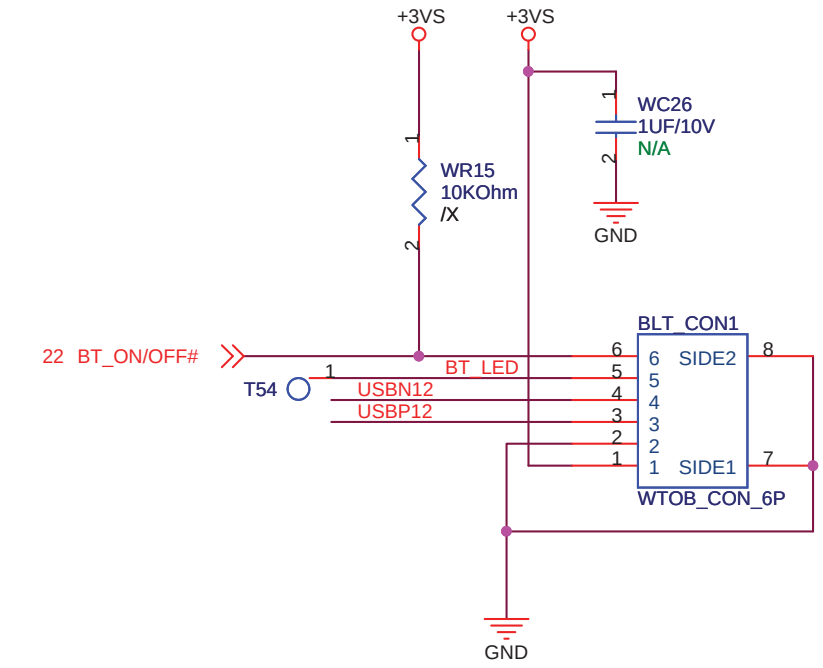
Title : HDMI

ASUSTek COMPUTER INC

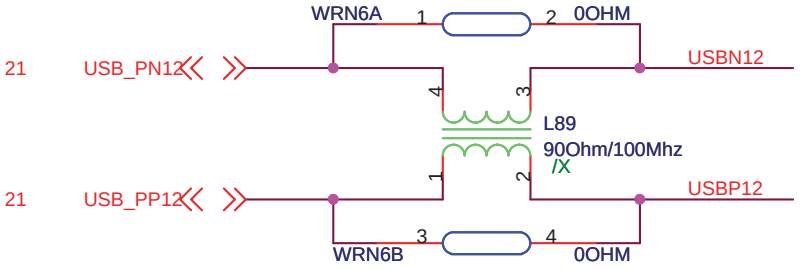
Engineer: N/A

Size	Project Name	Rev
A3	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 25 of 79

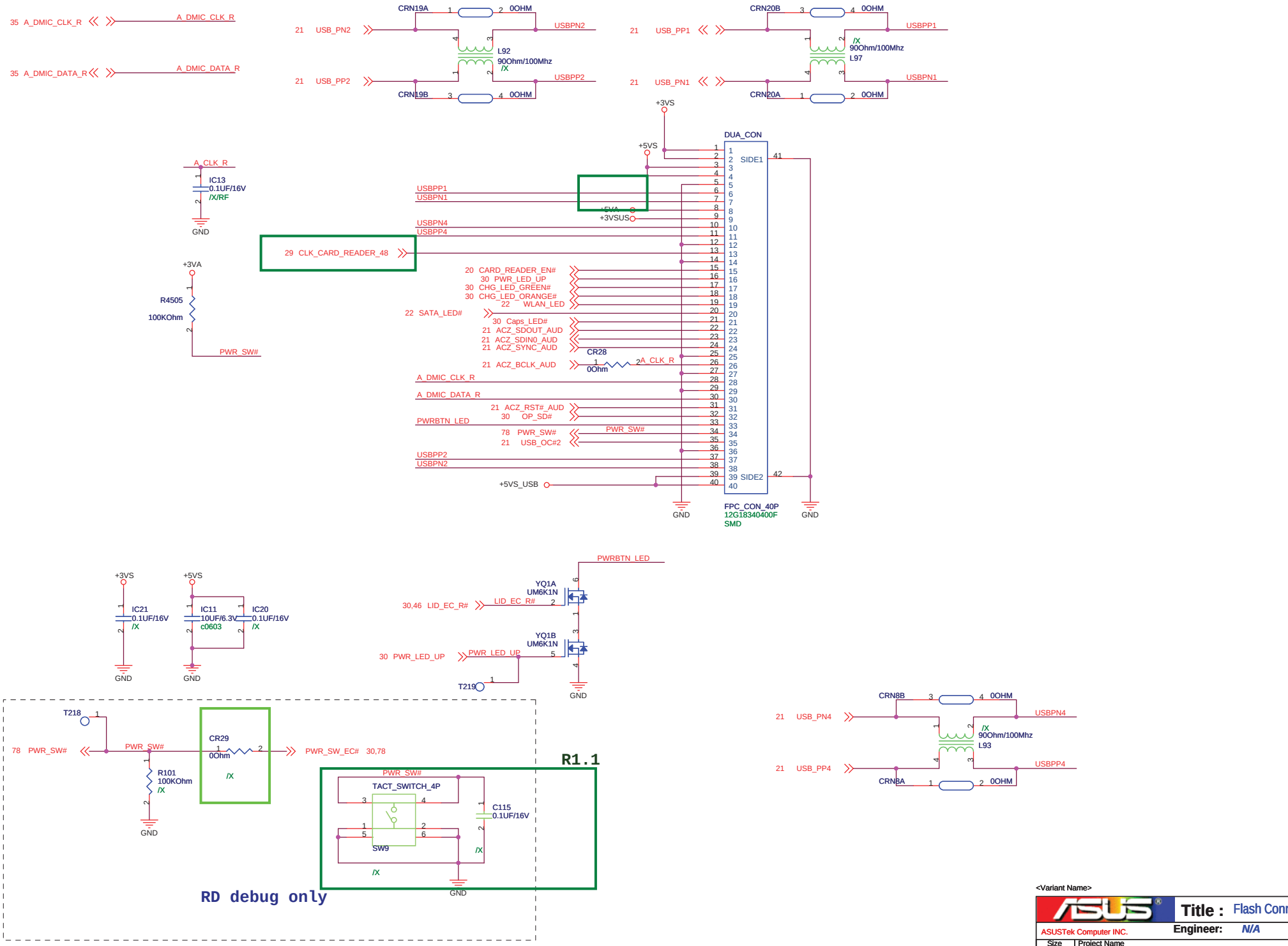


BT Conn



<Variant Name>

ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: N/A	
Size: A	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 27 of 79	



<Variant Name>

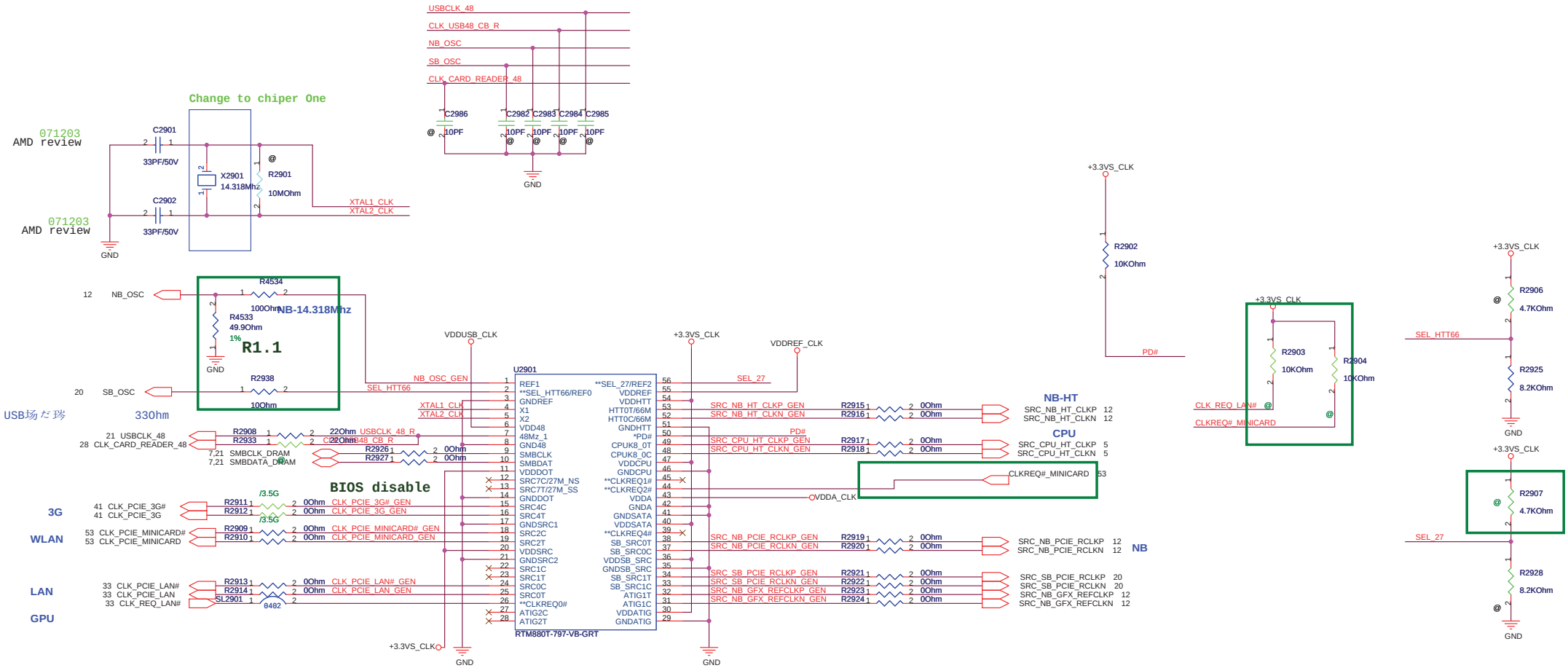
ASUSTek Computer INC.

Title : Flash Conn

Engineer: N/A

Size	Project Name	Rev
A3	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 28 of 79



SEL_27	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.

SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

<Variant Name>

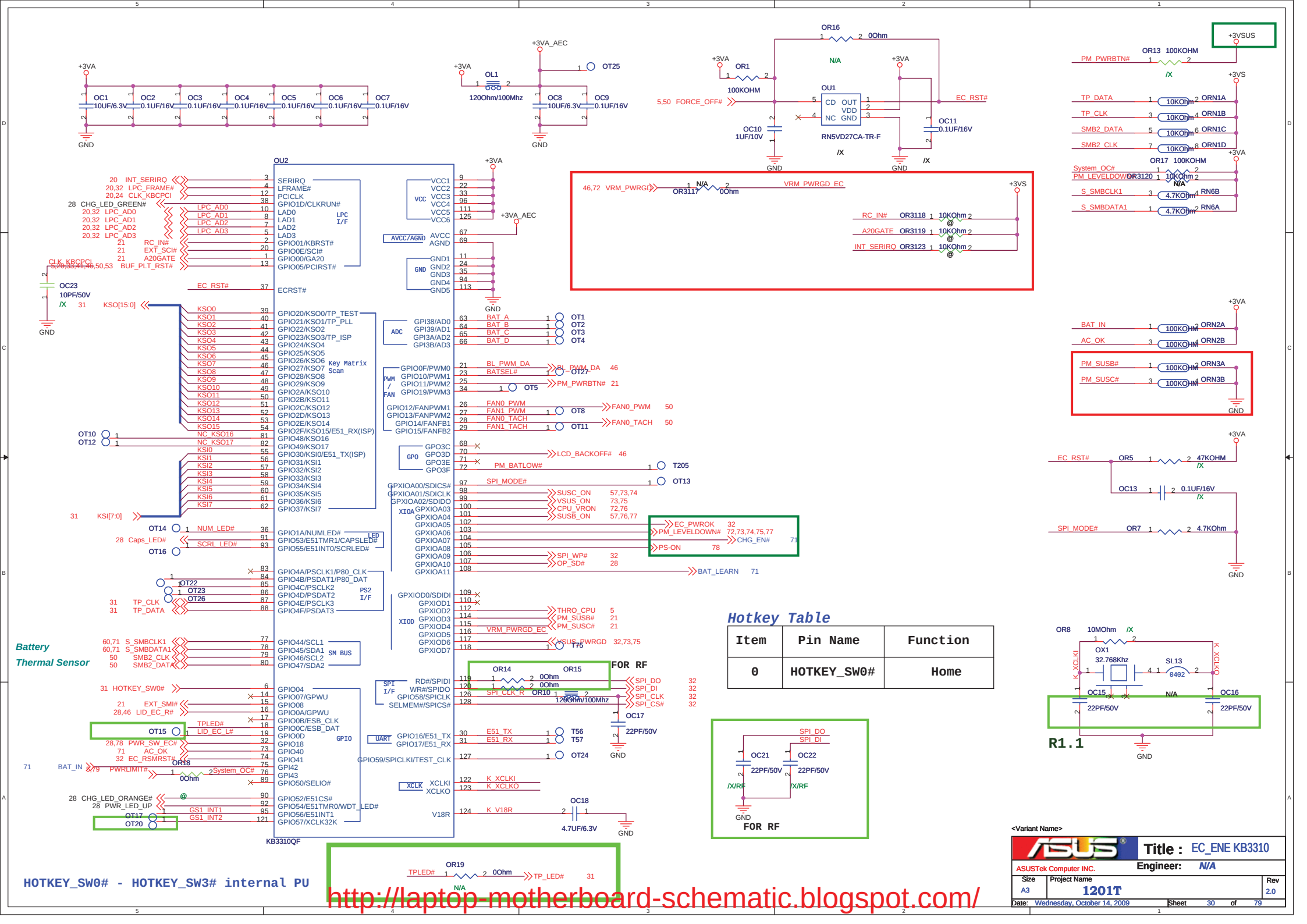
ASUSTeK COMPUTER INC

Title : RTM880T-797-VB-GRT

Engineer: N/A

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 29 of 79


OU2
KB3310QF
Key Matrix Scan
Battery
Thermal Sensor
FOR RF
FOR RF
HOTKEY_SW0# - HOTKEY_SW3# internal PU
R1.1
Hotkey Table
Item | Pin Name | Function
0 | HOTKEY_SW0# | Home
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: N/A
Size A3
Project Name 1201T
Rev 2.0
Date: Wednesday, October 14, 2009
Sheet 30 of 79
http://laptop-motherboard-schematic.blogspot.com/

1201HA need check pin define

CON2 12G182102402

FPC_CON_24P

For Keyboard Connector

KSO[15:0] 30

KSI[7:0] 30

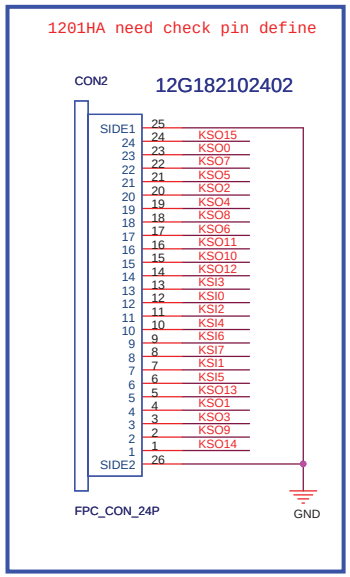
FOR RF and EMI

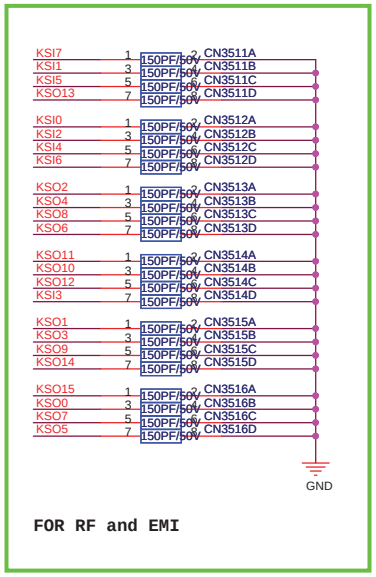
R1.1 change to 150pf

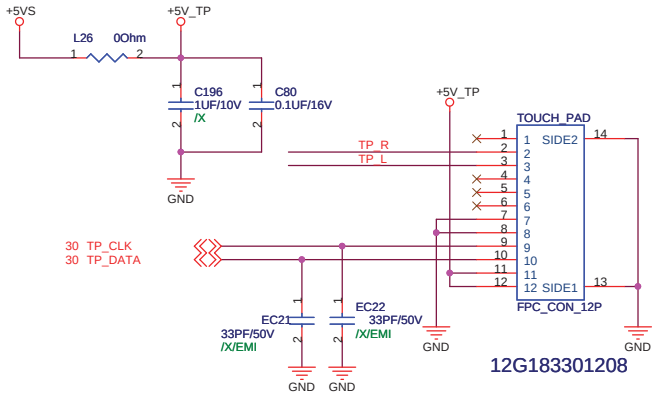
8/3 Del Keyboard ESD Protect

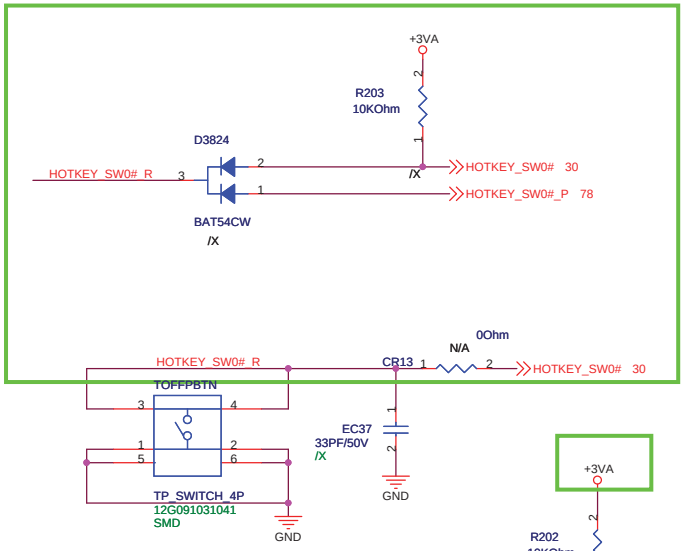
For Touch-Pad

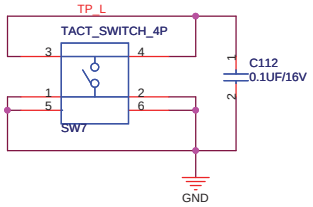
12G183301208

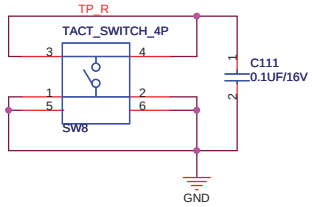


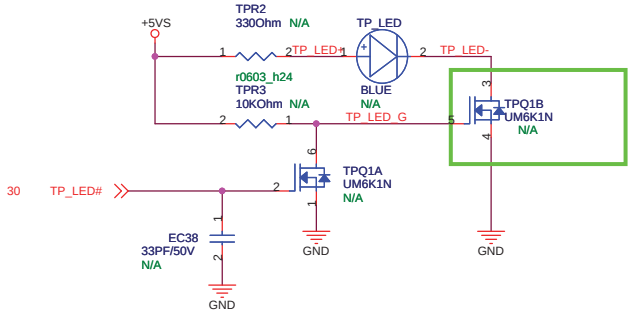












<Variant Name>

ASUSTek Computer INC.

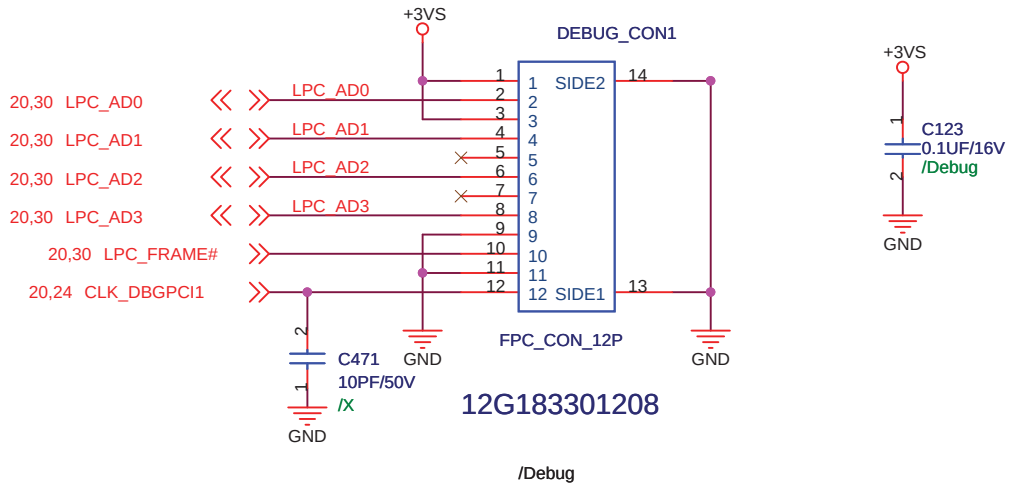
Title : KB_Touch Pad

Engineer: N/A

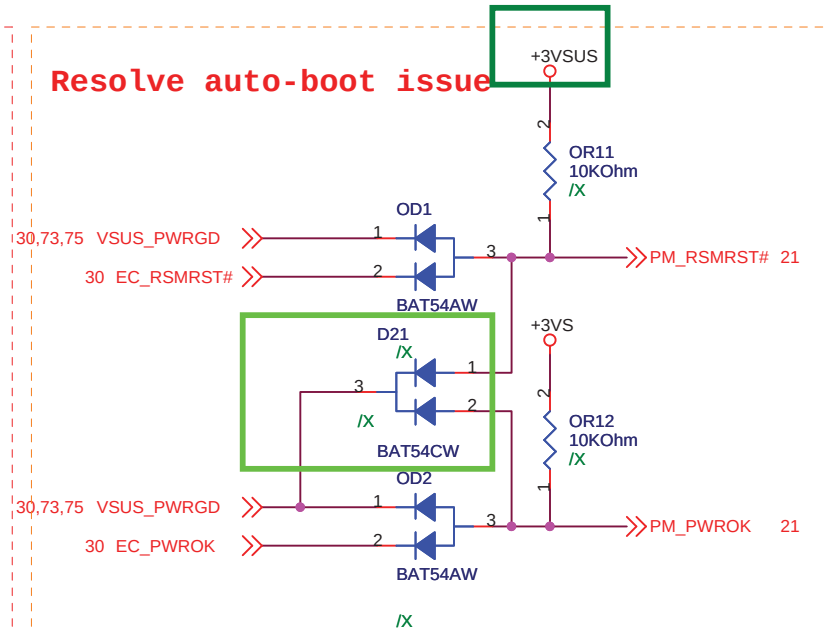
Size	Project Name	Rev
A3	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 31 of 79

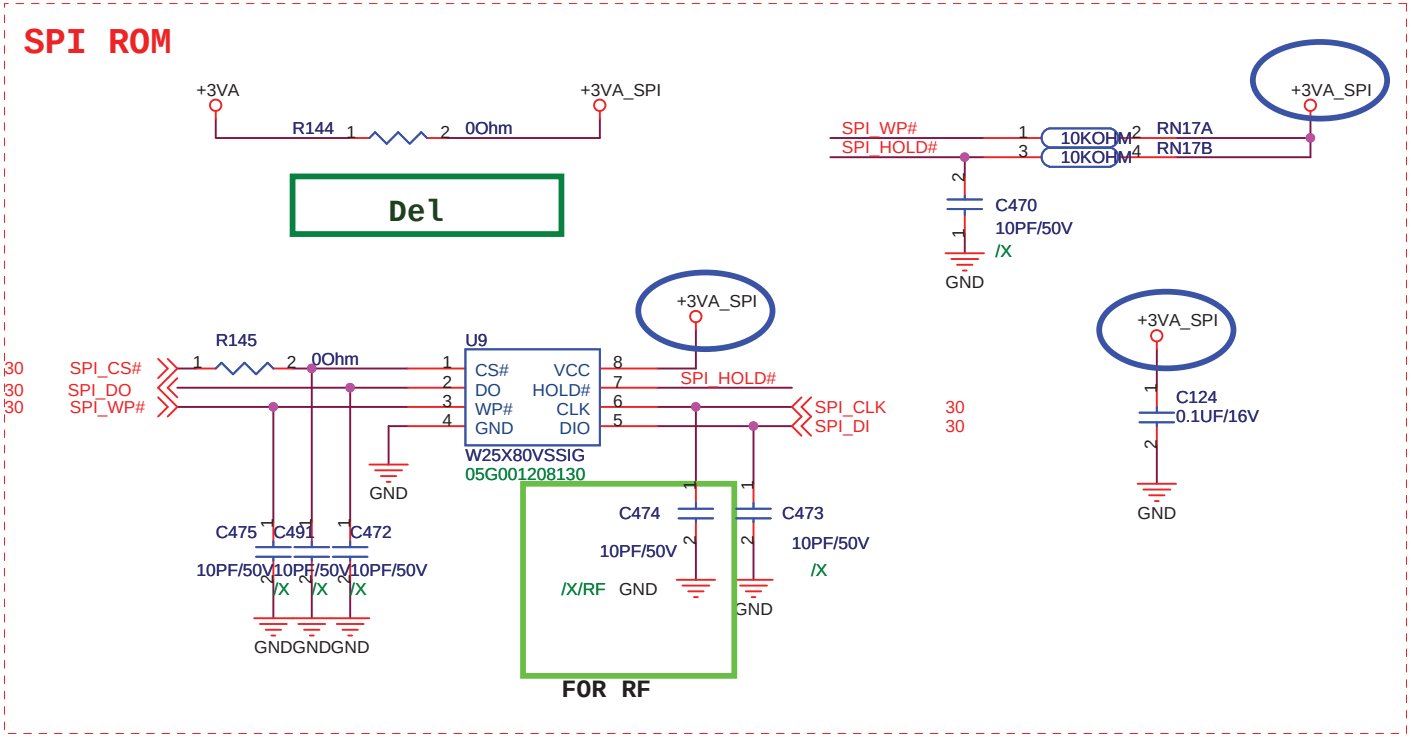
For Debug

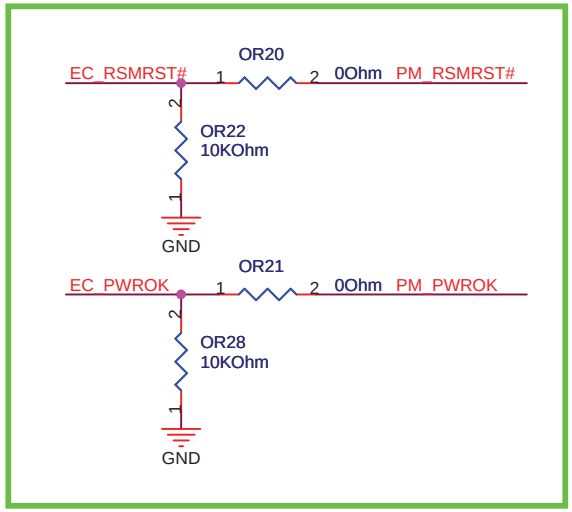


Resolve auto-boot issue



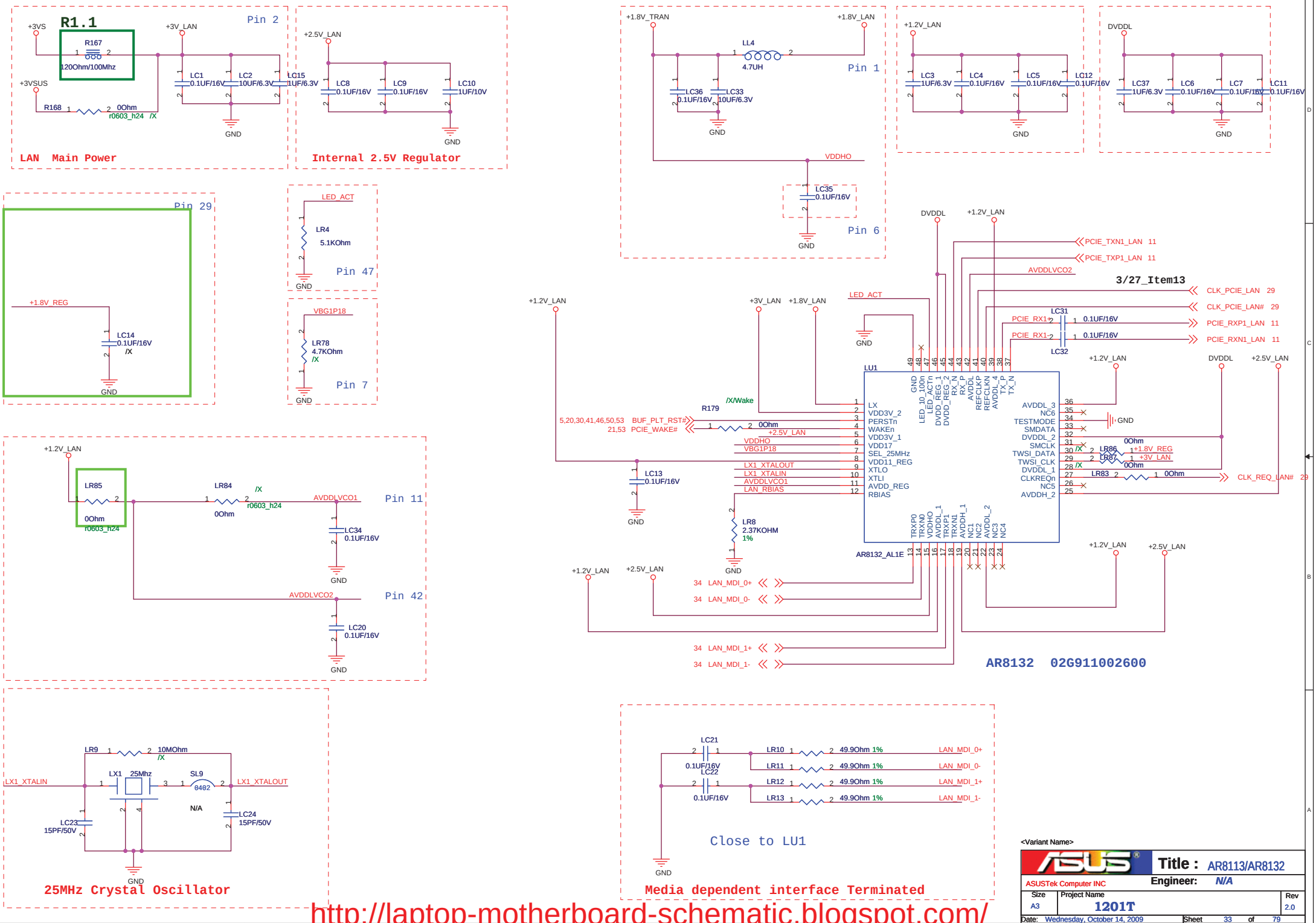
SPI ROM

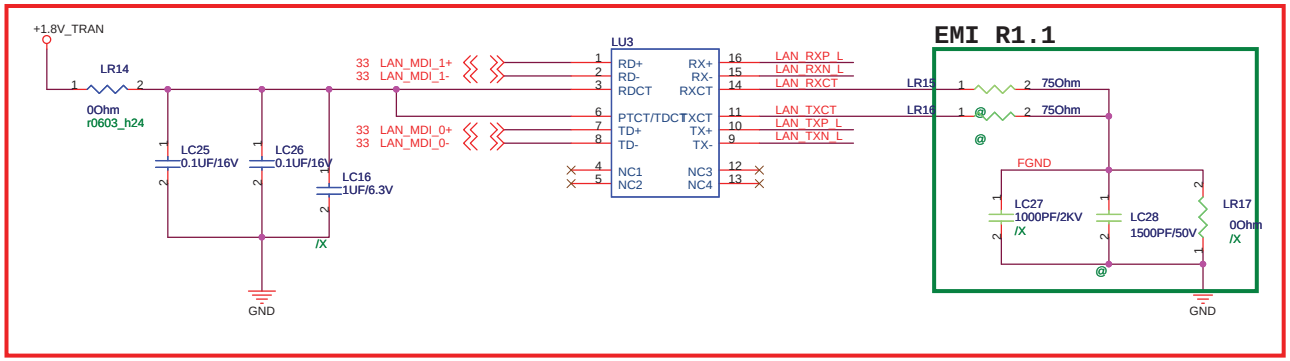


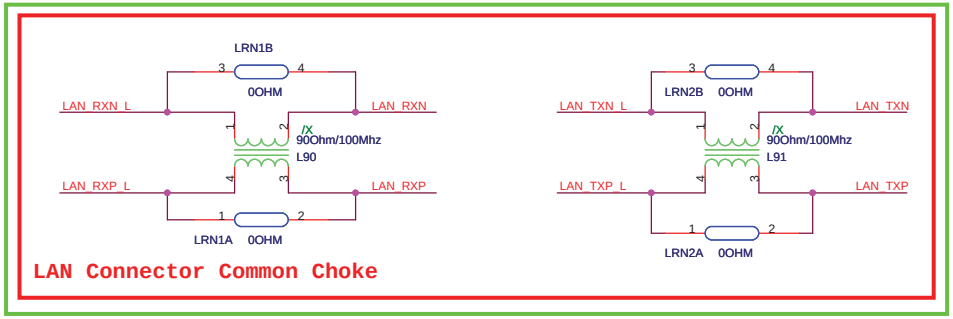


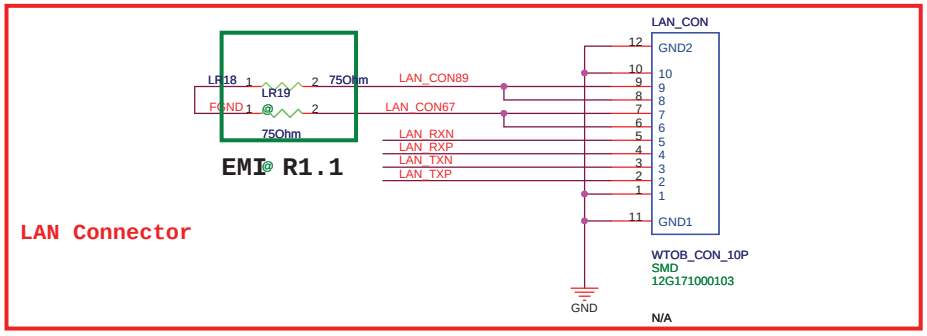
<Variant Name>

ASUSTek Computer INC.	Title : SPI ROM/ Debug	
	Engineer: N/A	
Size: A4	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 32 of 79	









<Variant Name>

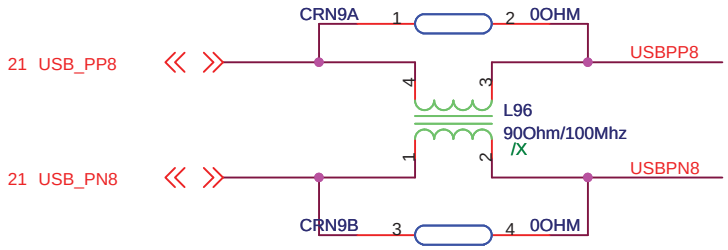
ASUSTek Computer INC.

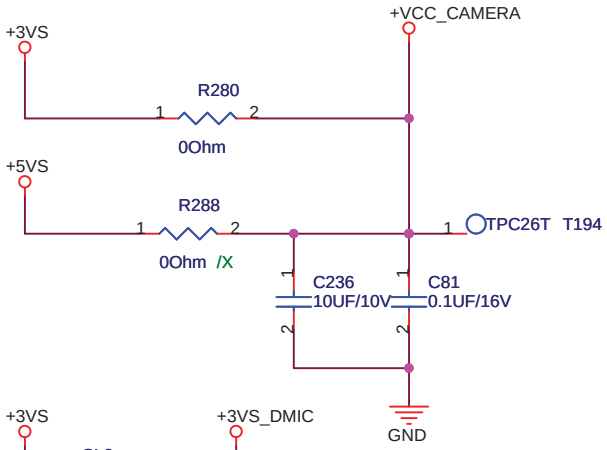
Title : RJ45

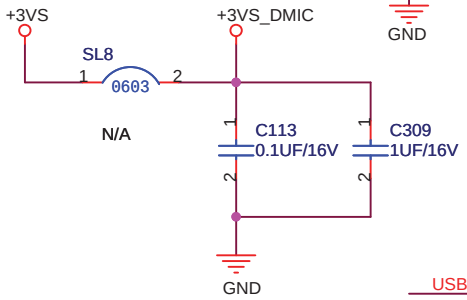
Engineer: N/A

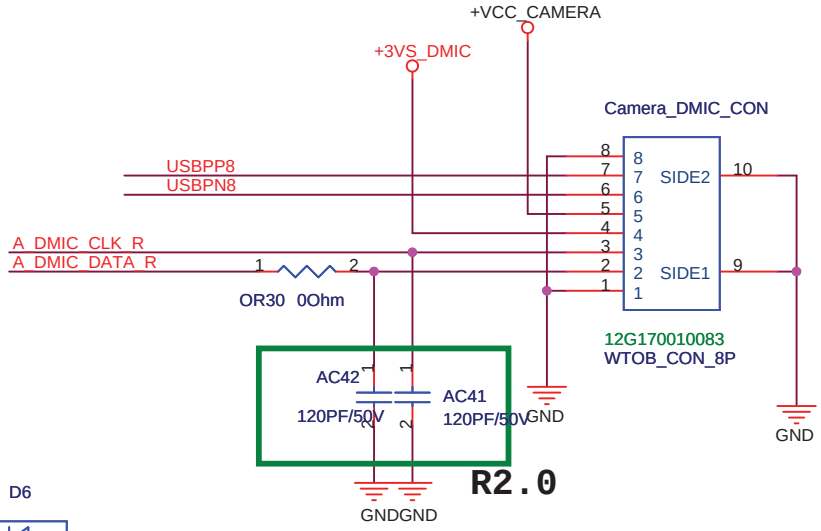
Size	Project Name	Rev
A3	1201T	2.0

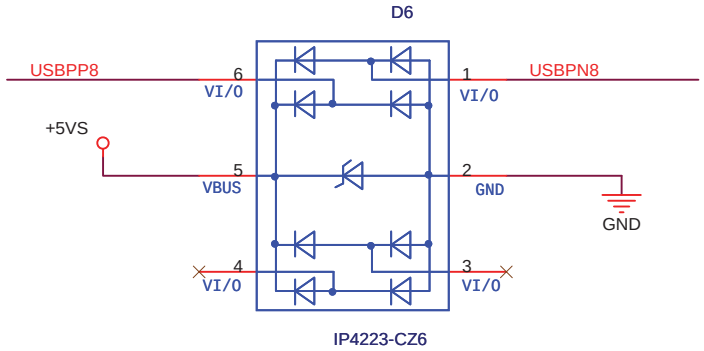
Date: Wednesday, October 14, 2009 Sheet 34 of 79











<Variant Name>

ASUSTek Computer INC.

Title : CMOS

Engineer: N/A

Size	Project Name	Rev
A4	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 35 of 79

<Variant Name>

ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: N/A	
Size: Custom	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 36 of 79	

<Variant Name>

Title : Bluetooth

ASUSTek Computer INC.

Engineer: N/A

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 37 of 79

<Variant Name>

Title : Bluetooth

ASUSTek Computer INC.

Engineer: N/A

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 38 of 79

<Variant Name>

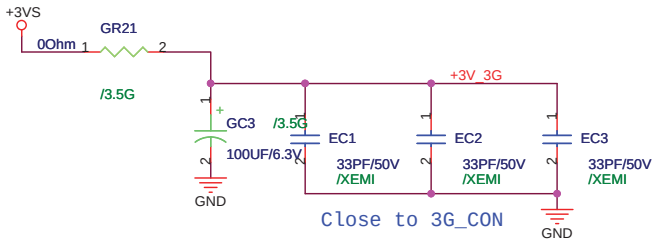
Title : CB_AU-6371_JEL

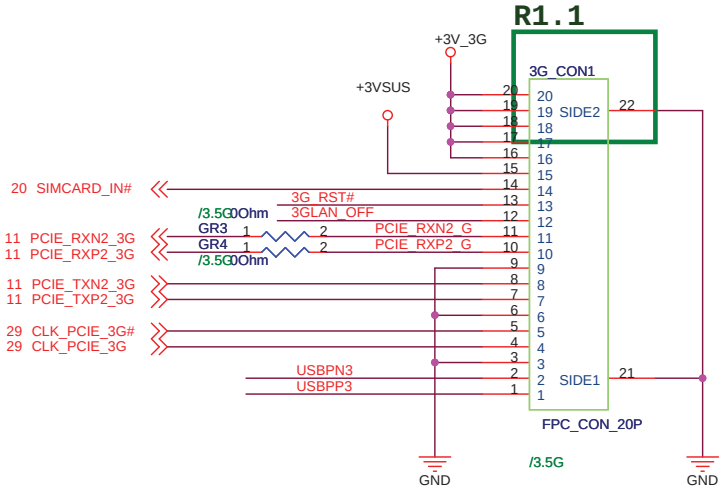
ASUSTeK COMPUTER INC

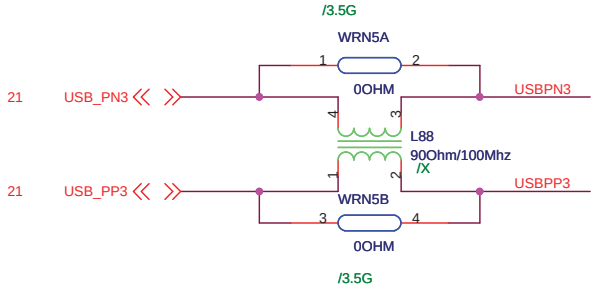
Engineer: N/A

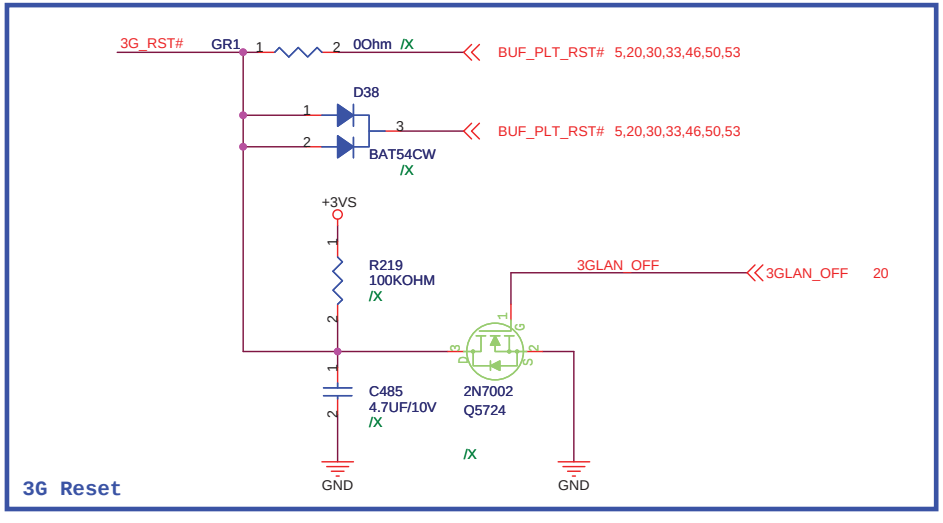
Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 40 of 79





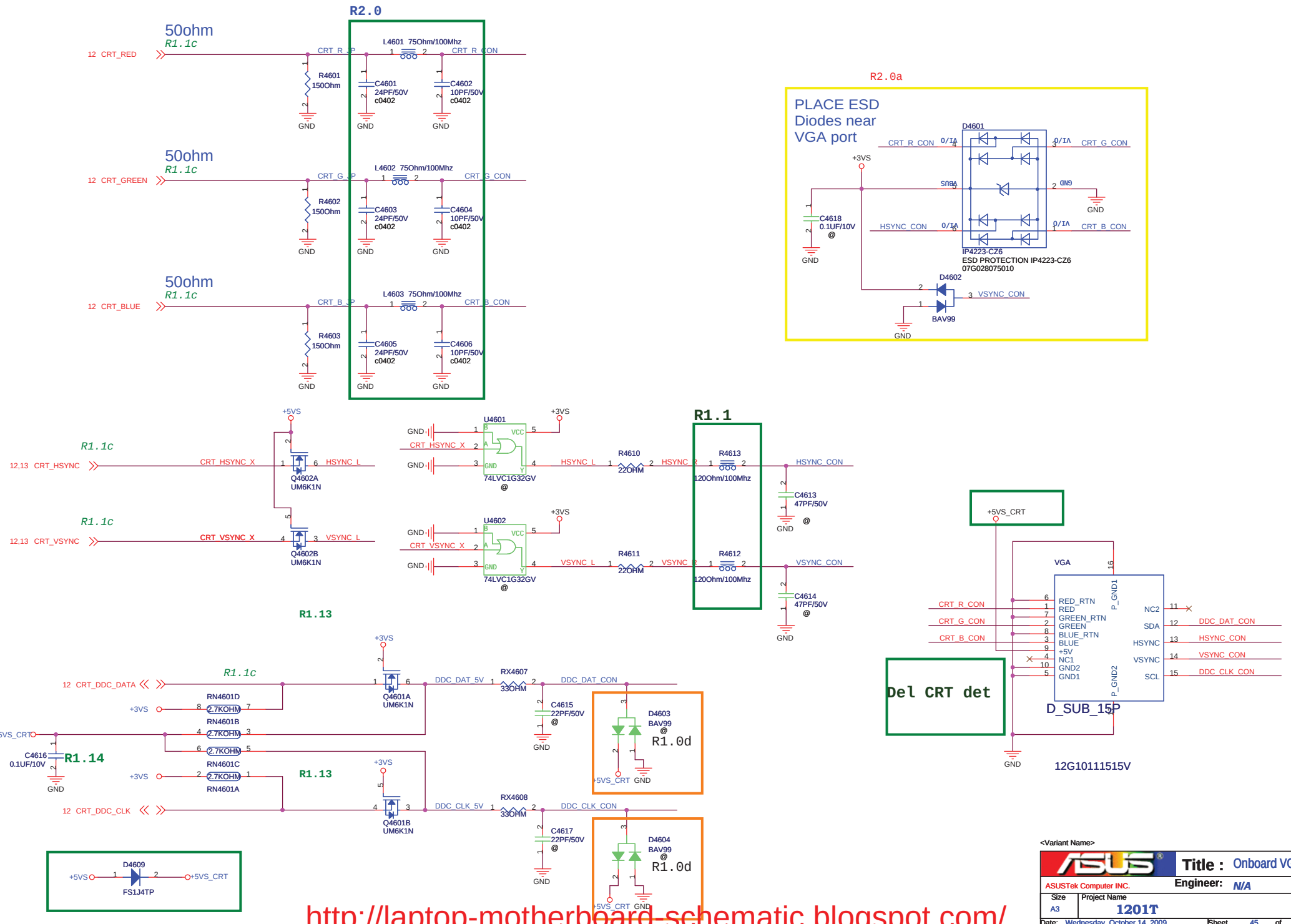


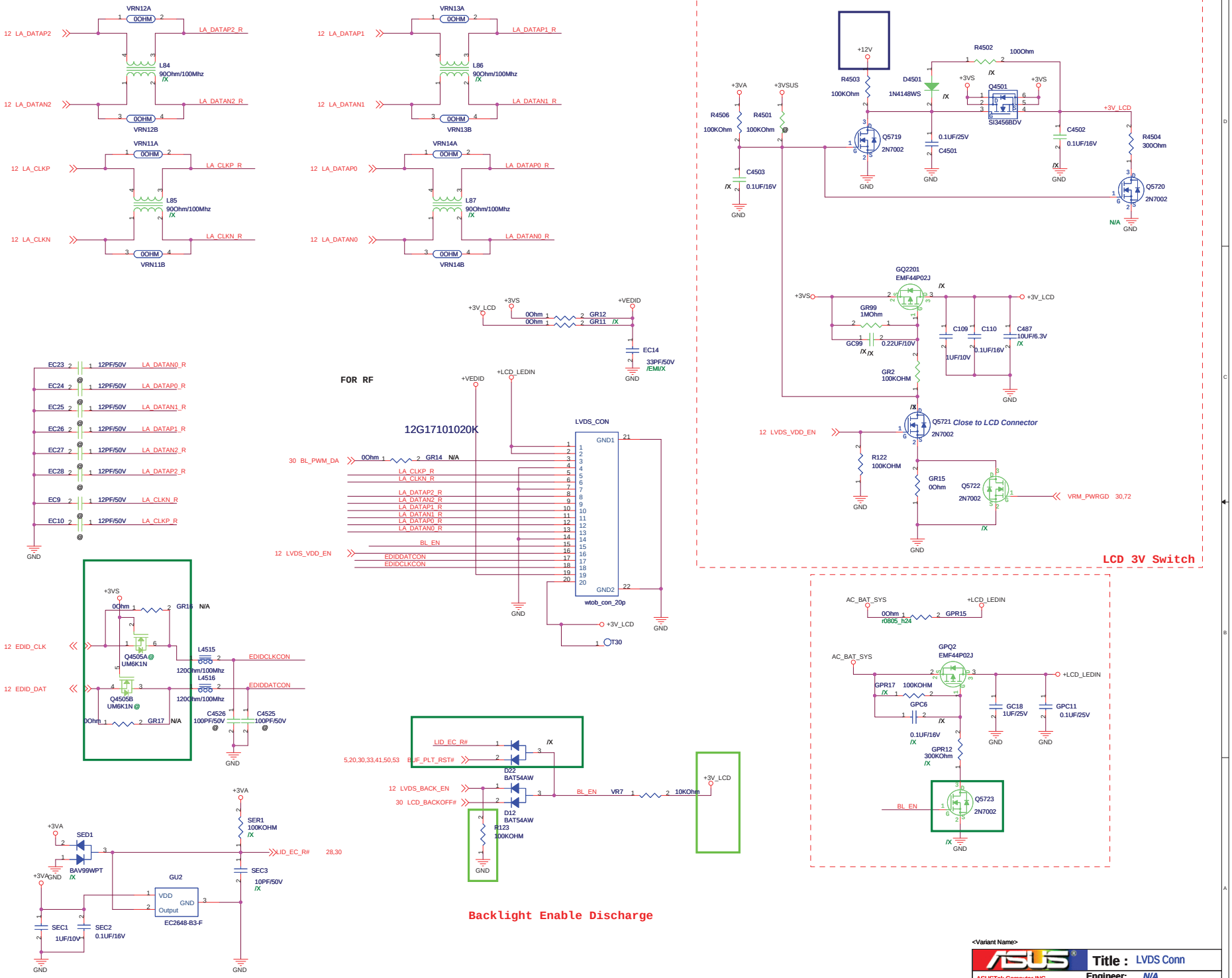


<Variant Name>

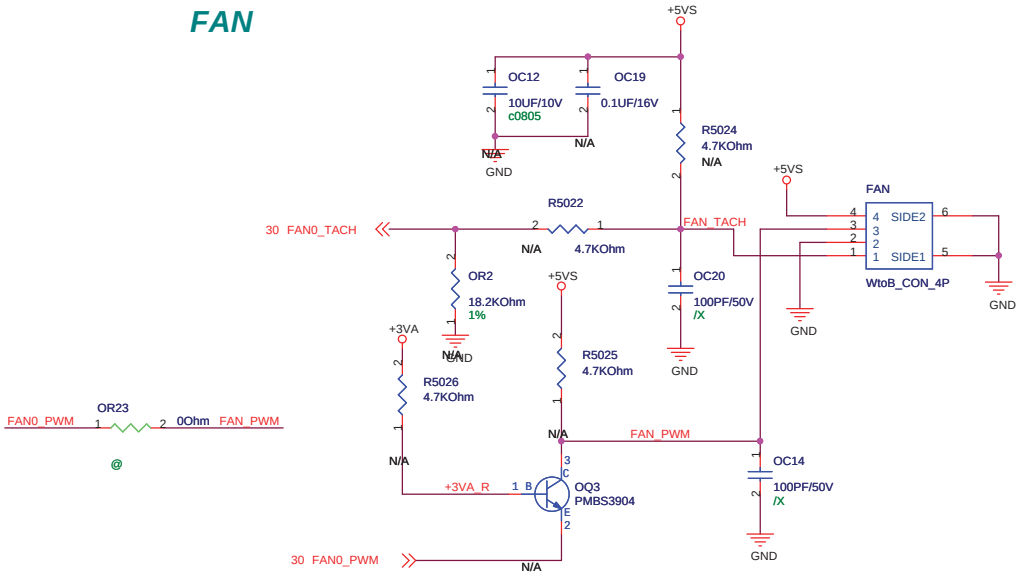
3.5G Module & External Antenna

ASUSTek Computer INC.	Title :	
	Engineer: N/A	
Size: Custom	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 21, 2009	Sheet 41 of 79	

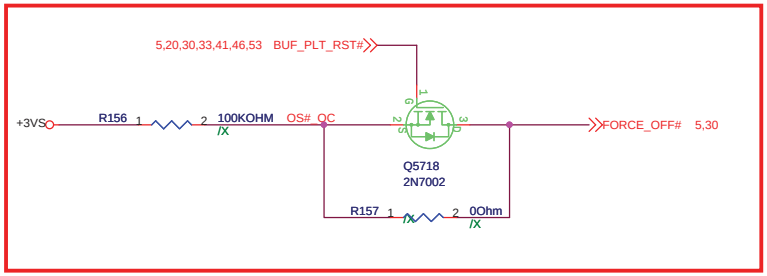


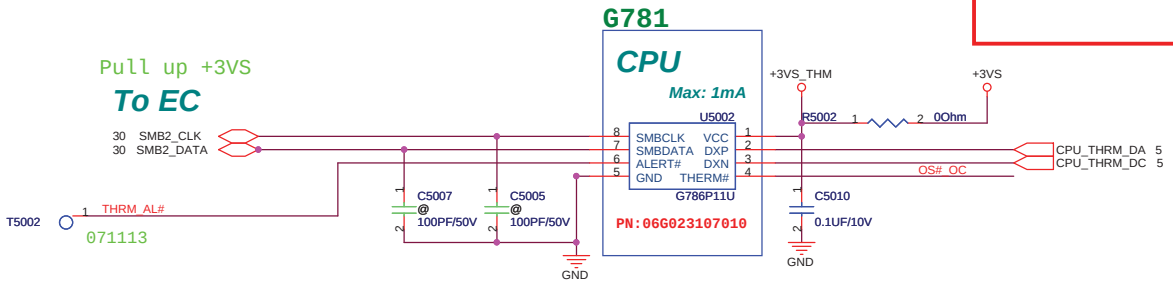


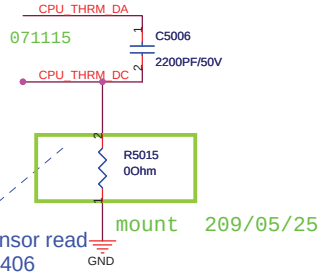
FAN



Thermal Sensor





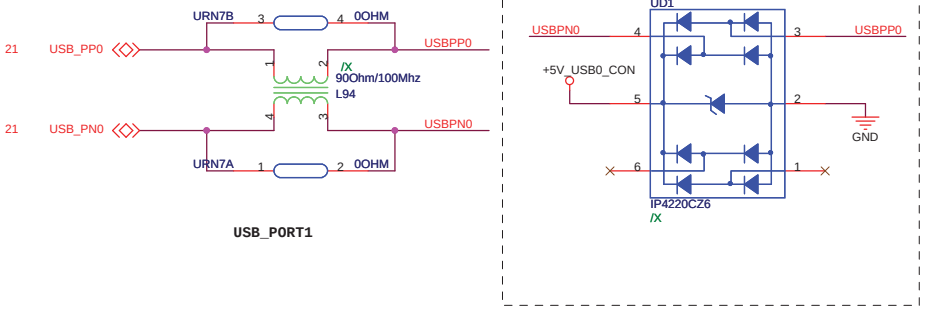


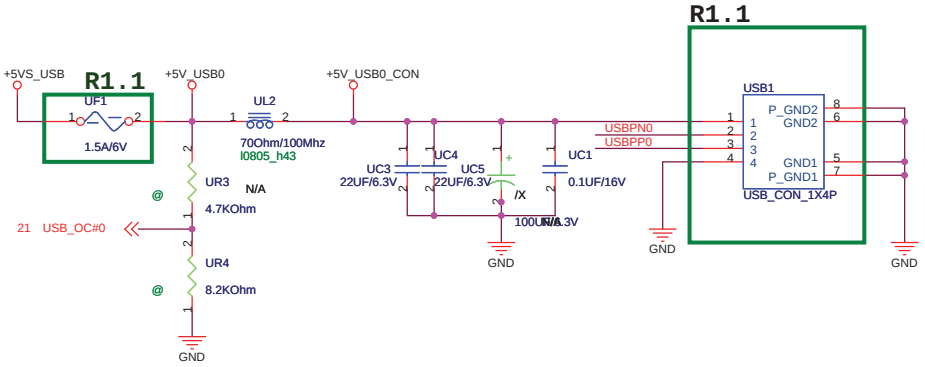
Add R5014 for thermal sensor read wrong temp issue. 090406

mount 209/05/25

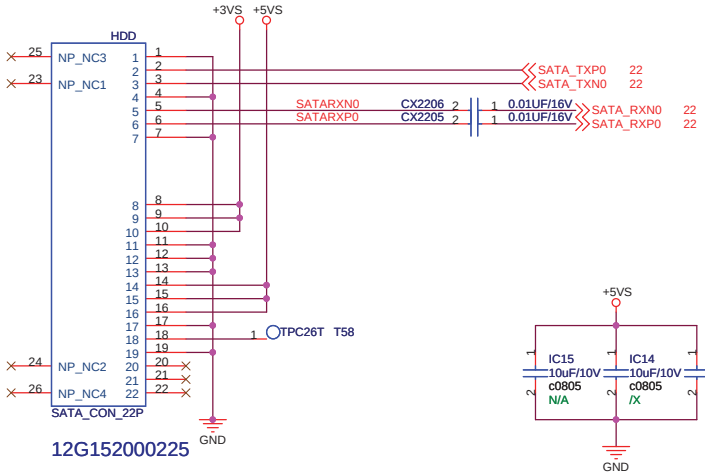
<Variant Name>

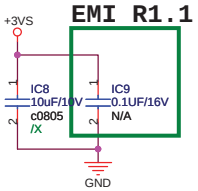
ASUSTek Computer INC.	Title : FAN_THERMAL SENSOR	
	Engineer: N/A	
Size: Custom	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 50 of 79	





SATA HDD Connector





<Variant Name>

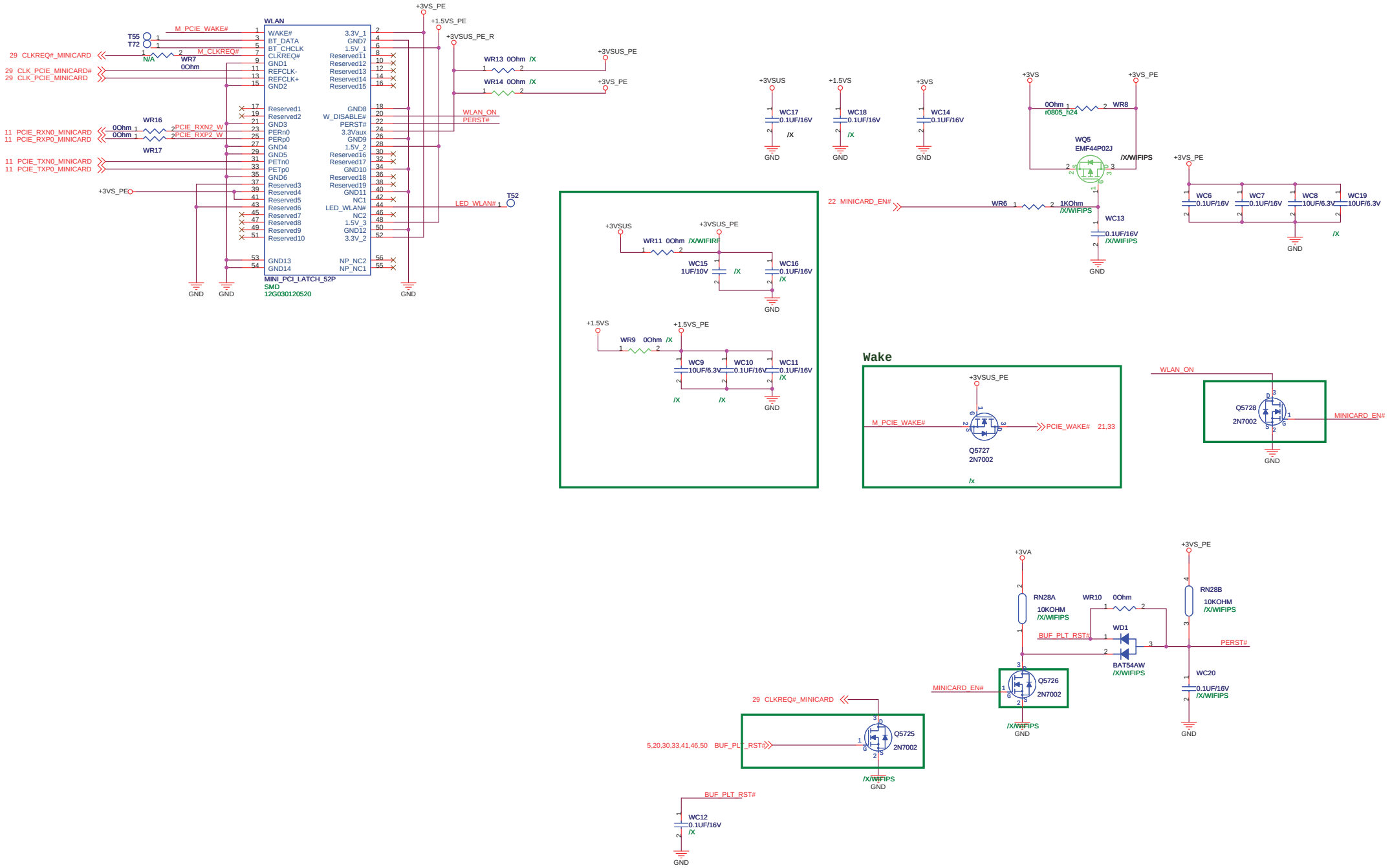
ASUSTek Computer INC.

Title : USB Port

Engineer: N/A

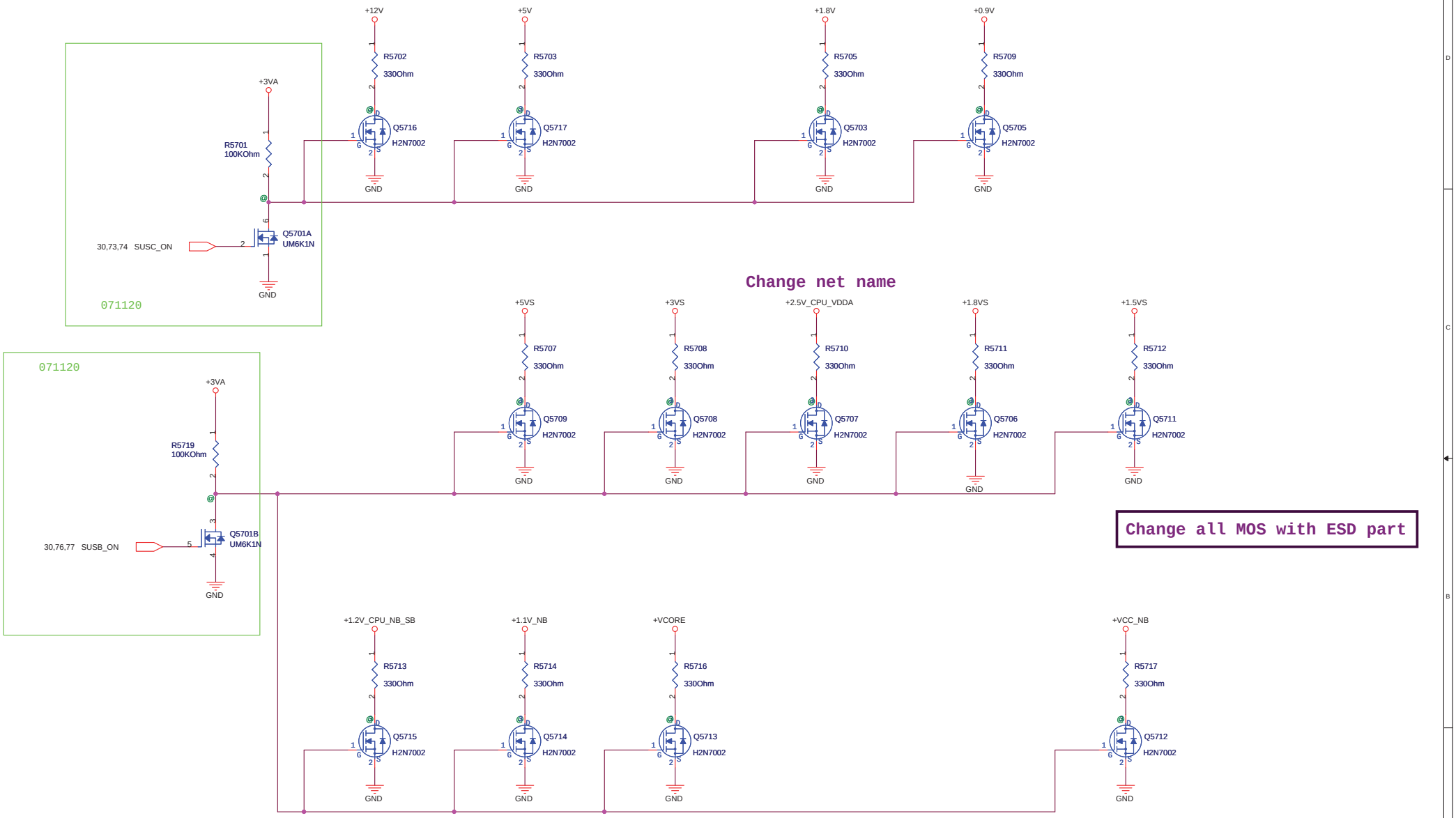
Size	Project Name	Rev
A3	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 52 of 79



<variant_name>

Title :	Mini WIFI
ASUSTek Computer INC.	Engineer: N/A
Size: Custom	Project Name: 1201T
Rev: 2.0	
Date: Wednesday, October 14, 2009	Sheet 53 of 79



<Variant Name>

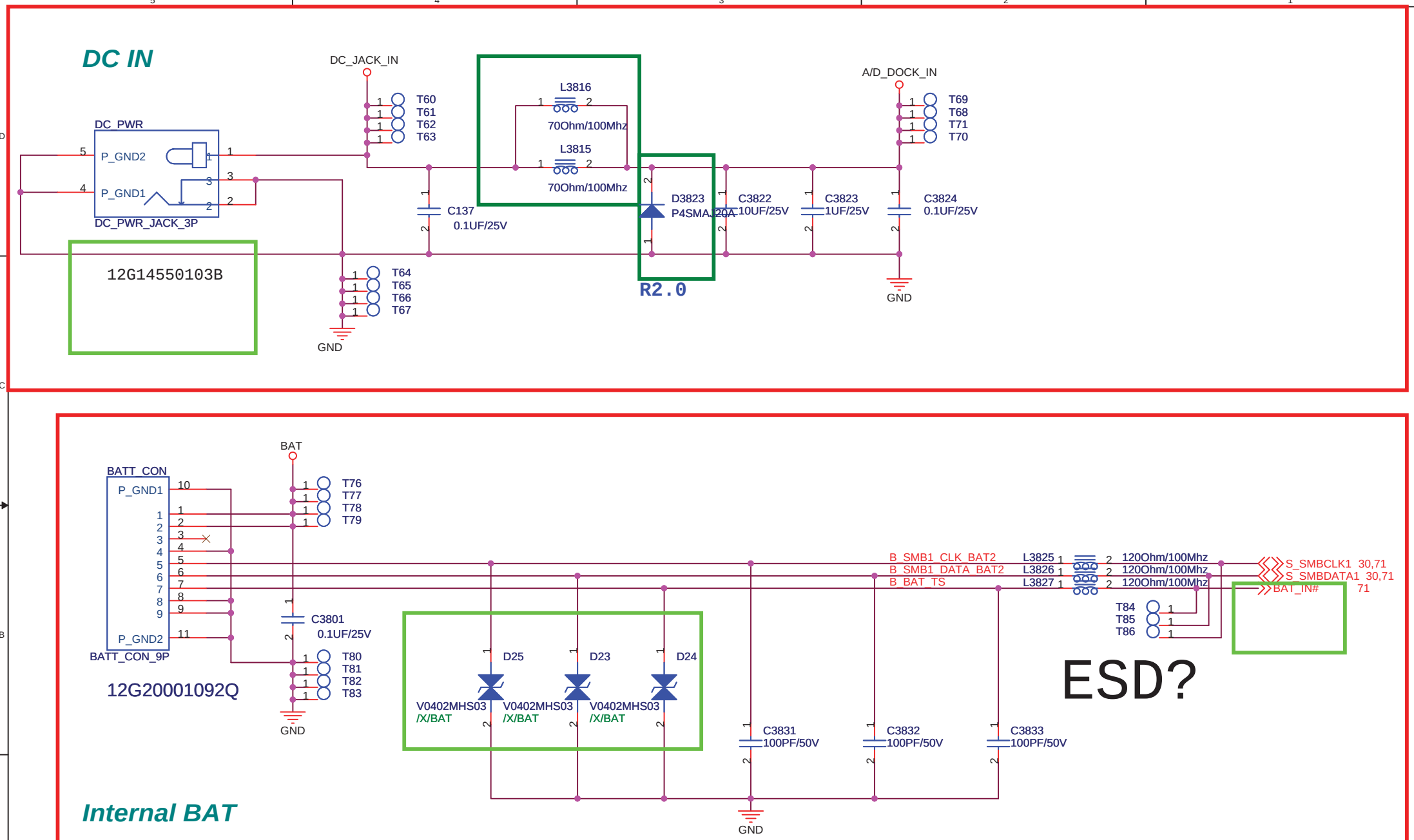
Title : DISCHARGE CKT

ASUSTeK COMPUTER INC

Engineer: N/A

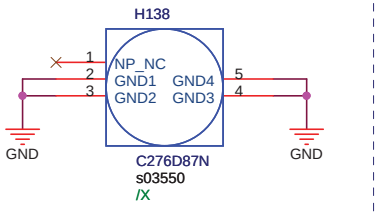
Size	Project Name	Rev
Custom	1201T	2.0

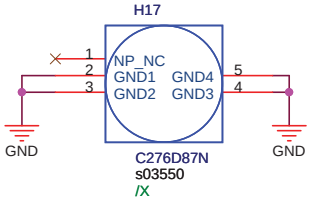
Date: Wednesday, October 14, 2009 Sheet 57 of 79

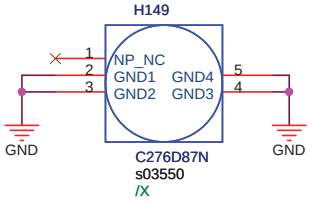


<Variant Name>

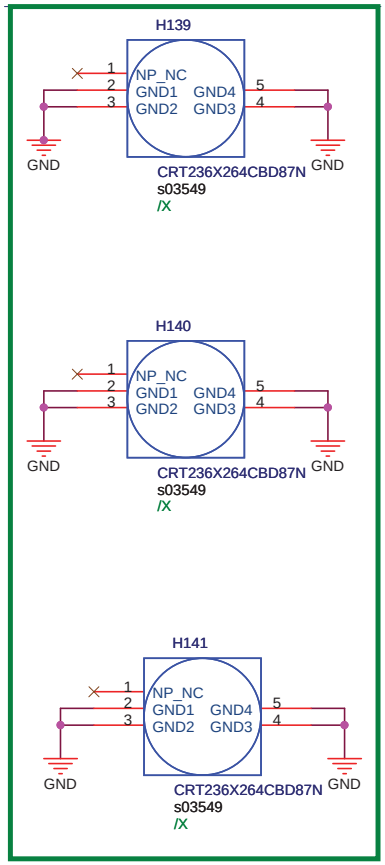
ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: N/A	
Size: A4	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 60 of 79	

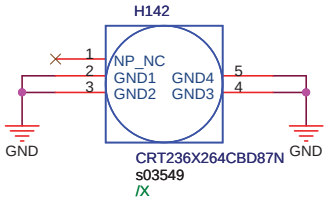


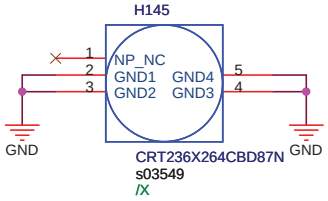




Detail B



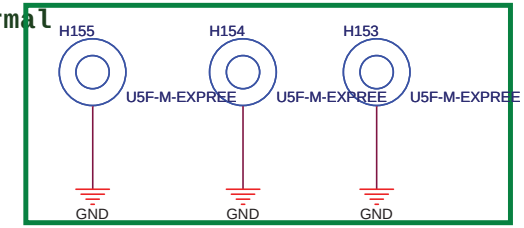


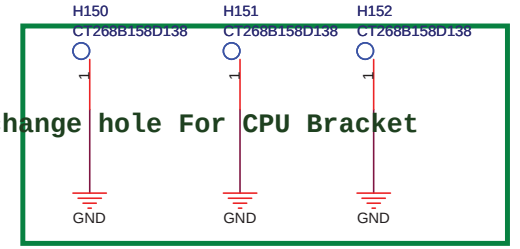


Detail C/Detail B

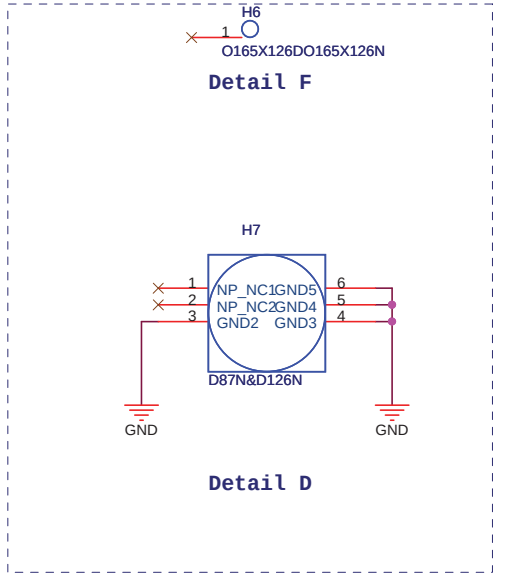
For Thermal

Detail A



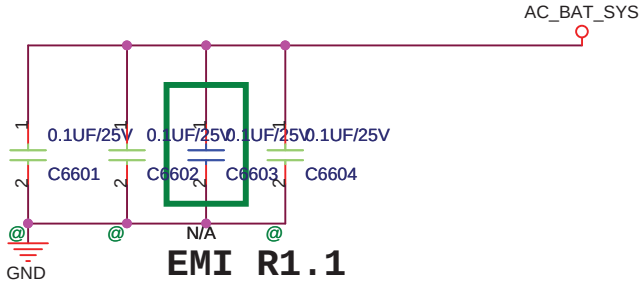


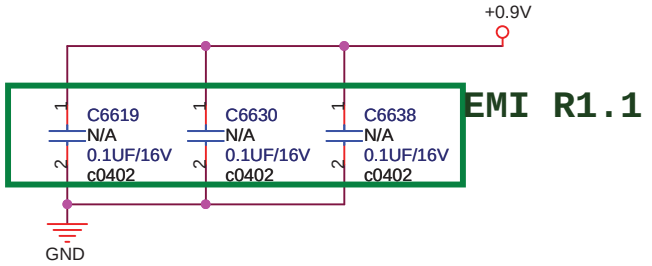
R1.1 change hole For CPU Bracket

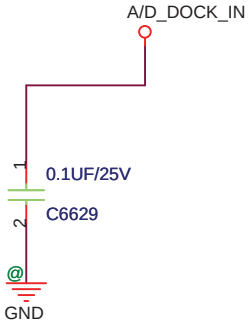


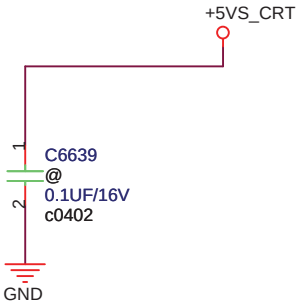
<Variant Name>

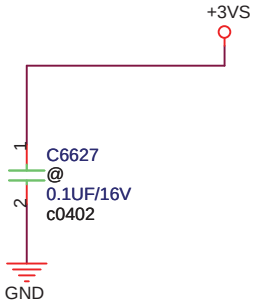
ASUSTek Computer INC.	Title : Screw Hole		
	Engineer: N/A		
Size: Custom	Project Name: 1201T		Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 65 of 79		

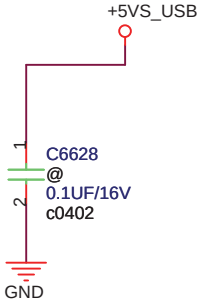












<Variant Name>

ASUSTeK COMPUTER INC

Title : EMI

Engineer: N/A

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 21, 2009 Sheet 66 of 79

R1.0

8/14: change DC-in jack to 12G14550103B
add 1.8VS power for sideport

8/17: Swap DDR address for layout request
add cap for EMI request

8/18: Swap DDR address for layout request
P33 del CLK_25M_LAN
P60 change L3815 to other parts,add L3816
add L1211

8/19: P50 change FAN CON and some related components
P12 change LVDS BL enable singal LVDS_BACK_EN, del L_G_BKLT_CTRL

R1.1

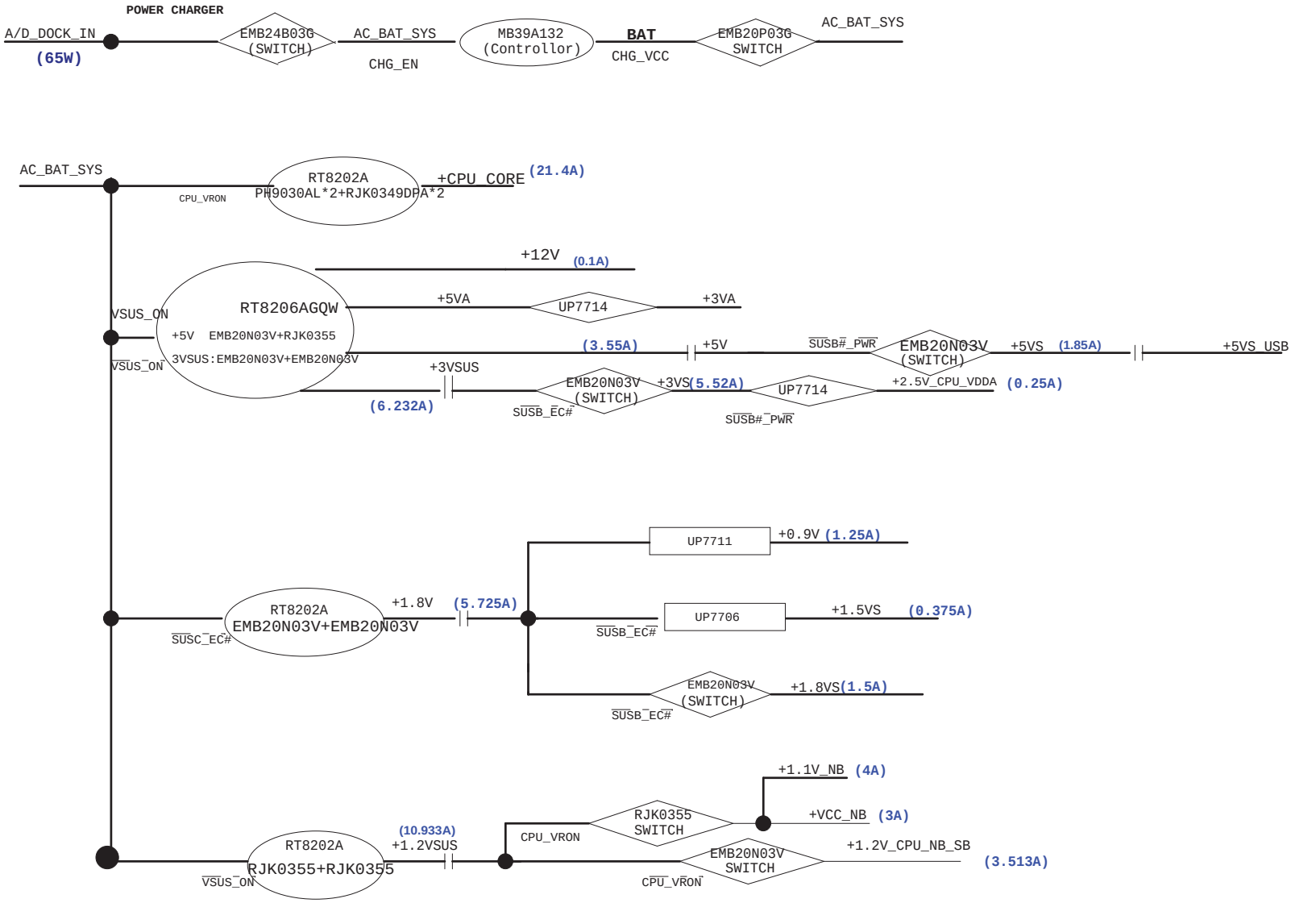
1.change 3G_CON to 3G_CON1
2.H150，H151，H152 no need NUT, and change hole size
3.OC15 OC16 change to 22pf
4.UF1 fuse change to 07G014150121
5.R4612，R4613 change to 120ohm/100Mhz bead for EA test
6.R2104 change to 8.87K 10G213887113030 for EA
7.mount C2913，C2917 ，add C2945， change R2938 to 22ohm;
change R4534 to 100Ohm, R4533 to 49.9Ohm
8.change some parts for EMI request
9.VDDHTTX 与CPU_VLDT分别预留0 ohm到+1.1V_NB
10. CN3511-CN3516 change to 150pf array CAP
11.Unmount SW9，C115
12.change R2938 to 10ohm,
13.change R167 to 120Ohm/100Mhz bead for noise test
14.USB1 change Part Number to 12G13107004E
15. unmount L0301,mount L0302; unmount L1403,mount L1405;

R2.0

1. DMIC:AC41, AC42 change to 120pf CAP
2. P45 CRT:C4601/C4603/C4605：24PF/50V
L4601/L4602/L4603：75Ohm/100Mhz Bead
C4602/C4604/C4606：10PF/50V
3. change D3823 to a TVS diode

<Variant Name>

ASUSTek Computer INC.	Title : History	
	Engineer: N/A	
Size: A	Project Name: 1201T	Rev: 2.0
Date: Wednesday, October 14, 2009	Sheet 68 of 79	



STD version :1.00g(08/05/09)

<Variant Name>

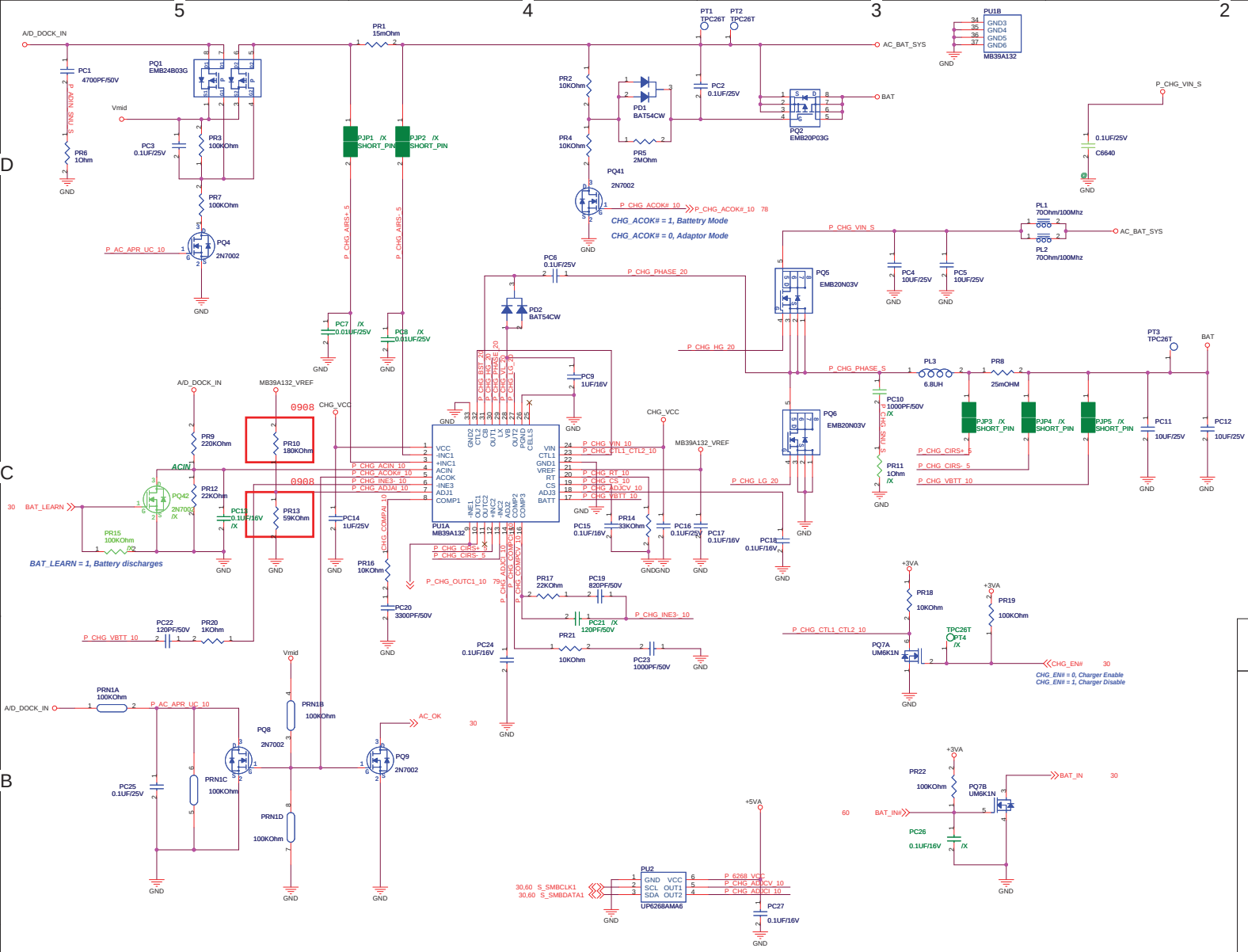
Title : Power_FLOW

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A2		2.0

Date: Thursday, October 15, 2009 Sheet 70 of 79



Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.64A
2. Ripple Current:
   I ripple =0.875A
   I spec=2A ⊙1 pcs
3. Inductor Spec:
   I sat=8 A
   I dc =4.5A
   DCR=60mohm
4. MOSFET Spec:
   H-side MOSFET: EMB20N03V
   Rds(ON)= 23 mohm (Vgs=5 V)
   I cont = 6A (T =25)
   I peak = 32 A
   L-side MOSFET: EMB20N03V
   Rds(ON)= 23 mohm (Vgs=5 V)
   I cont = 6A (T =25)
   I peak = 32 A

Controller

1. Voltage & Current:
   +12.6V@2.5A
2. Frequency:
   PR14=33KOHM,
   Fosc=17000/RT(Kohm)=515KHz
3. OCP:
4. POR:
   POR Hysteresis =0.1V
   V on =7.5V
5. Enable Voltage:
   V = 2.9 V
6. Soft start time:
   Tss=23ms
7. Phase selection:
   N/A
8. Inrush Current:
   C total =20uF
   I inrush= 0.01A

Battery Charging Current :

Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

VREF = 5.0V

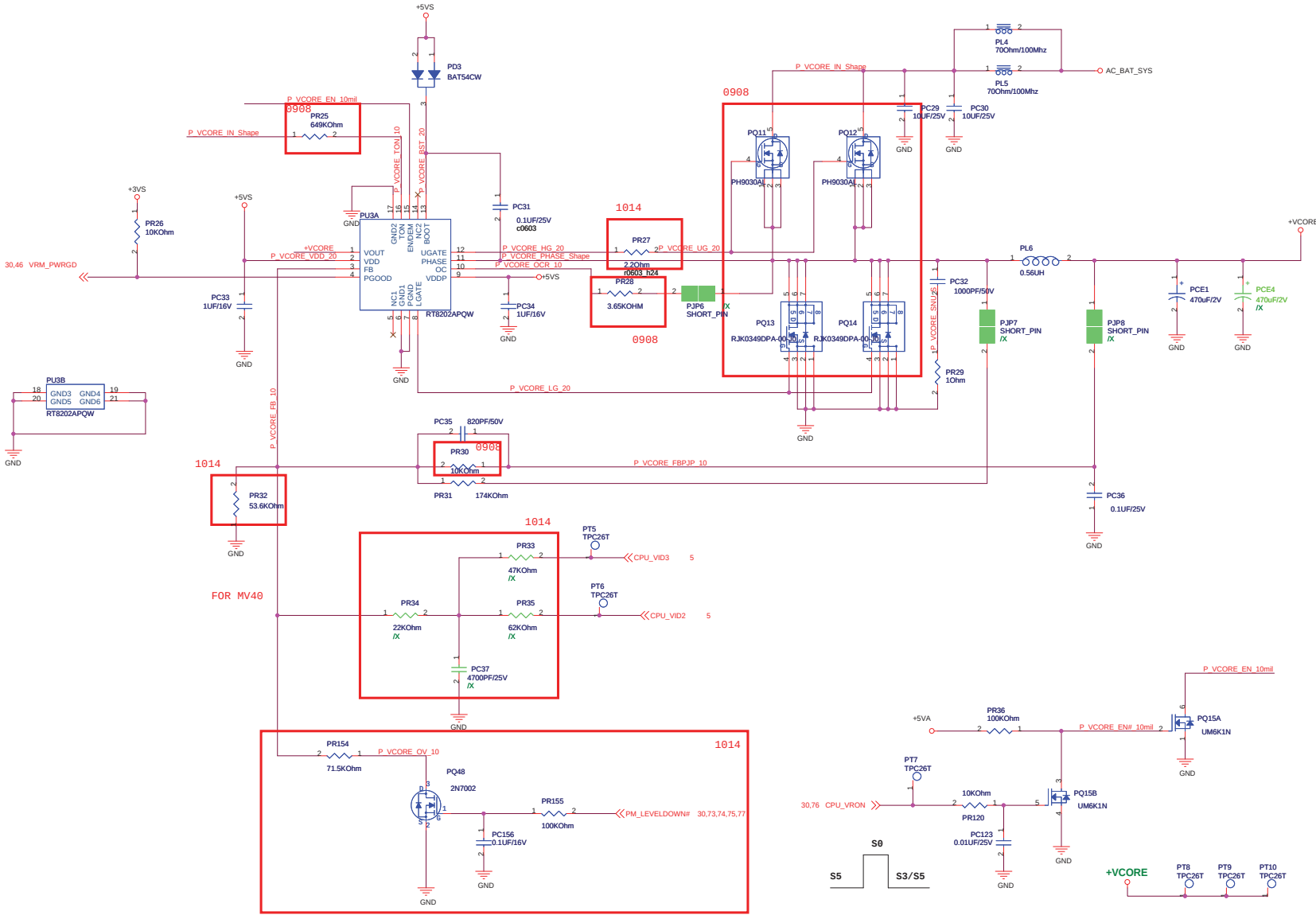
fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.23 * CS (uF)*

<Variant Name>

ASUSTek Computer INC

Title : Charger
Engineer: N/A
Size A2 | Project Name 1201T | Rev 2.0
Date: Wednesday, October 21, 2009 | Sheet 71 of 79



Controller

1. Voltage & Current:
   VCORE: 18A
2. Frequency:
   Ton=3.85p*Rt(on)*Vout/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   SetPR28=6.34K
   Iocp=Rocp*20/Rds(on)=20*6.34/3.8=31.6A
4. Soft start time:
   Soft-Start duration is 1.35ms
5. Inrush Current:
   C total =470UF
   I inrush=0.35A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =2.5A
2. Ripple Current:
   Iripple=5.66A
3. Dynamic:
   Ipeak=18A
   ESR=9mohm
   V=162mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.6mohm
5. MOSFET Spec:
   L-side MOSFET: RJK0353DPA-00-J0
   Rds(on)max=7.6mOhm (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)

   H-side MOSFET: RJK0355DPA-00-J0
   WPAK
   Rds(ON)= 11.8 mohm (Vgs=4.5 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

FOR MV40

PM_LEVELDOWN#	VID3	VID2	Voltage
0	0	0	/
0	0	1	0.90V
0	1	0	/
0	1	1	/
1	0	0	/
1	0	1	1.00V
1	1	0	/
1	1	1	/

FOR L335

PM_LEVELDOWN#	VID3	VID2	Voltage
0	0	0	1.10V
0	0	1	0.95V
0	1	0	0.90V
0	1	1	0.75V
1	0	0	1.14V
1	0	1	1.00V
1	1	0	0.94V
1	1	1	0.80V

<Variant Name>

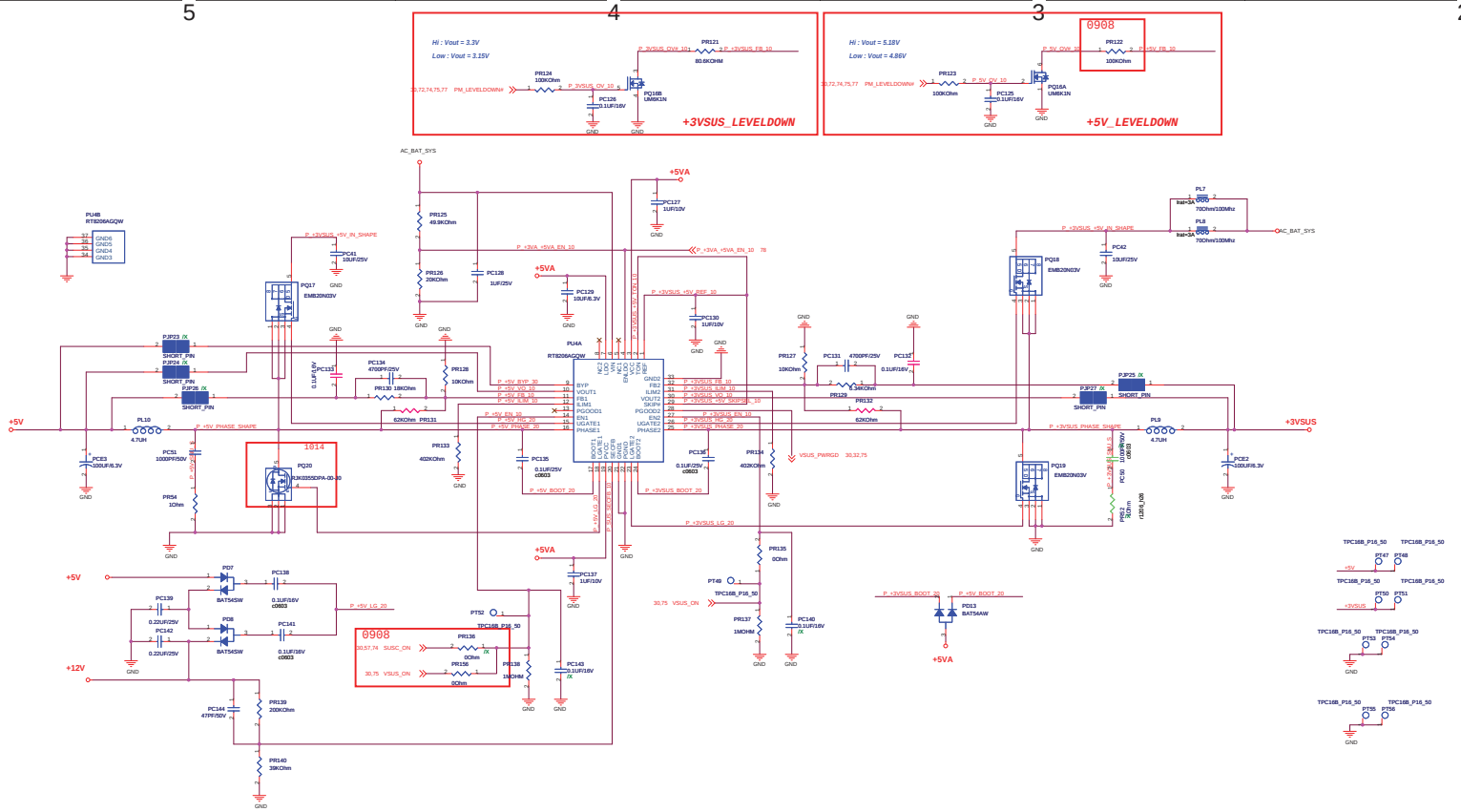
ASUSTeK COMPUTER INC

Title : Power_VCORE

Engineer:

Size	Project Name	Rev
C	1201T	2.0

Date: Thursday, October 15, 2009 Sheet 72 of 79

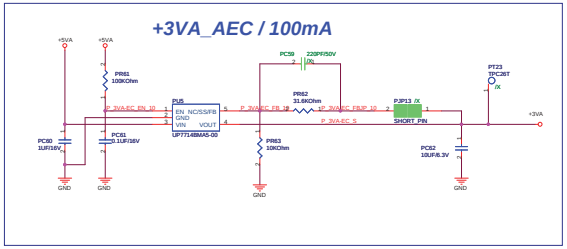


Power stage	+3VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =1.832A	
2. Ripple Current:	
I rip =1.92A	
I spec=2.5A	
1 pcs	
3. Dynamic:	
I peak=4A	
ESR / 1 pcs =18 mohm	
V =72mV	
4. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
5. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm (Vgs=4.5 V)	
I cont = 8 A (T =25)	
I peak = 32A (Pause 10 us)	
L-side MOSFET: EMB20N03V	
Rds(ON)= 23 mohm (Vgs=4.5 V)	
I cont = 8 A (T =25)	
I peak = 32 A (Pause 10 us)	

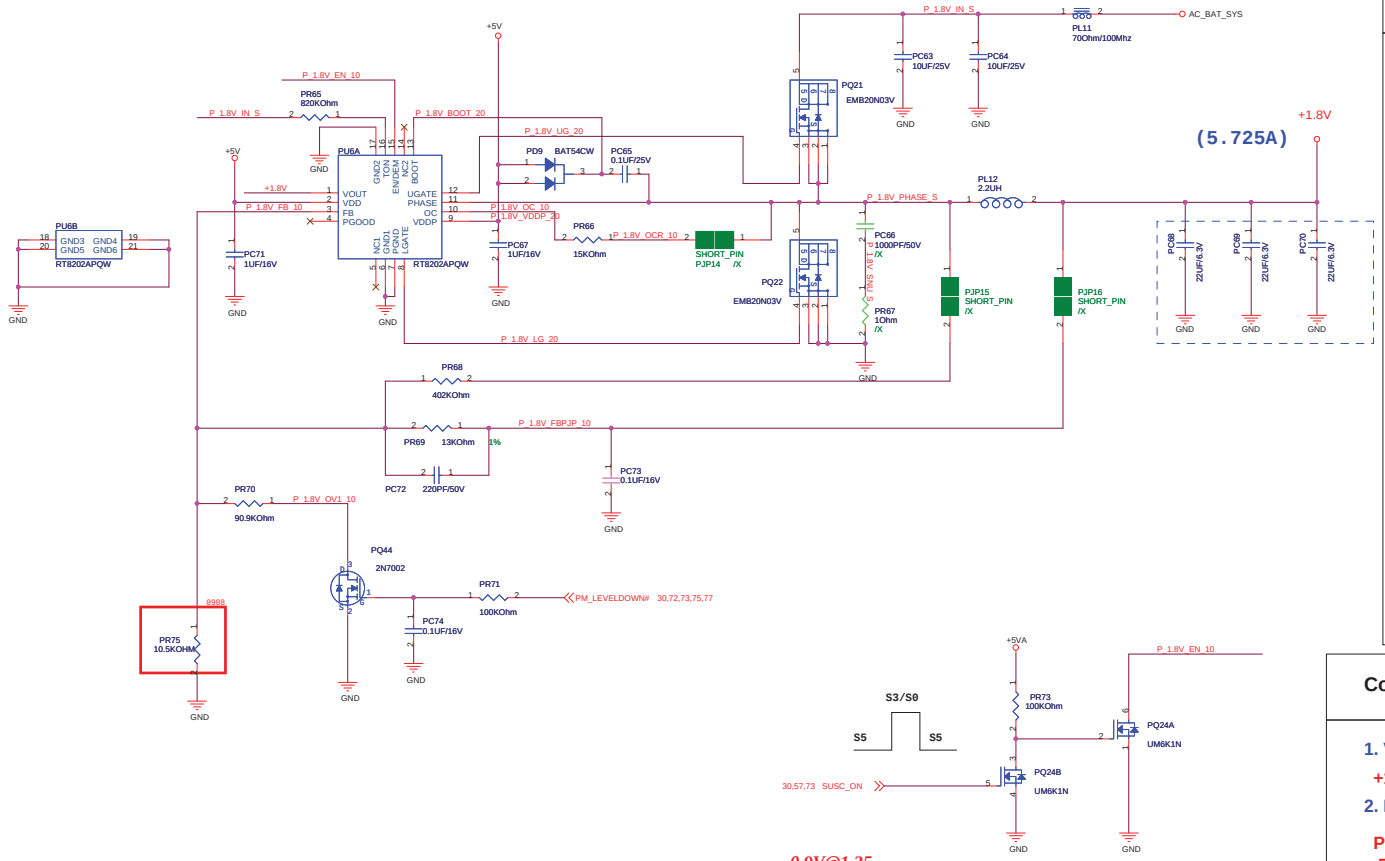
Power stage	+5VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =2.082A	
2. Ripple Current:	
I rip =1.482A	
I spec=2.5A	
1 pcs	
3. Dynamic:	
I peak=3A	
ESR / 1 pcs =18 mohm	
V =54mV	
4. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
5. MOSFET Spec:	
H-side MOSFET: SI7326DN_T1_E3	
Rds(ON)= 23 mohm (Vgs=4.5 V)	
I cont = 8 A (T =25)	
I peak = 32 A (Pause 10 us)	
L-side MOSFET: RJK0355DPA-00-J0 WPAK	
Rds(ON)= 11.8 mohm (Vgs=4.5 V)	
I cont = 30 A (T =25)	
I peak = 120 A (Pause 10 us)	

Controller	+3VSUS	Controller	+5VSUS
1. Voltage & Current:	6. OVP:	1. Voltage & Current:	6. OVP:
+3VSUS=3.3V@4A	V ovp=115%Vout	+5VSUS=5V@3A	V ovp=115%Vout
2. Frequency:	7. Enable Voltage:	2. Frequency:	7. Enable Voltage:
fosc=375KHz	V rising = 1V	fosc=300KHz	V rising = 1V
3. OCP:	V falling = 0.4 V	3. OCP:	V falling = 0.4 V
Set PR134=402Kohm	8. Soft start time:	Set PR133=402Kohm	8. Soft start time:
Iocp=8.74A	Tss=2ms	Iocp=17A	Tss=2ms
4. POR:	9. Phase selection:	4. POR:	9. Phase selection:
V on =4.35-4.5 V	/X	V on =4.35-4.5 V	/X
V off =3.9-4.25 V	10.Inrush Current:	V off =3.9-4.25 V	10.Inrush Current:
5. UVP:	C total = 110 uF	5. UVP:	C total = 110 uF
V uvp= 70% Vout	I inrush= 0.165 A	V uvp= 70% Vout	I inrush= 0.275 A

1. Dropout Voltage: 5. EN Voltage:
V= 210mV (Io=300m A) V rising = 2 V
V falling = 0.8
2. Current Limit: 6. Supply Voltage:
I limit= 480mA Vcc=3.3V
3. Continue Current: 7. Inrush current:
I cont= 100mA Tss = 400us
4. Pd: C total = 10 uF
R thjc =5 C/W I inrush= 62.5 mA
Pd =0.4W



Title : Power +5SUS&+3VSUS&+12VSUS
Engineer: N/A
ASUSTeK Computer INC
Size: A1 Project Name: 1201T Rev: 2.0
Date: Thursday, October 25, 2012 Sheet 73 of 79



PM_LEVELDOWN#	Voltage	Status
L	1.70V	Power Saving
H	1.8V	Normal

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.43A
2. Ripple Current:
   I rip =2.29A
   I spec=2.5A ⊙2pcs
3. Dynamic:
   I peak=5.725A
   ESR / 1 pcs =18 mohm
   〉V =103mV
4. Inductor Spec:
   I sat=14 A
   I dc =8 A
   DCR=18 mohm
5. MOSFET Spec:

   H-side MOSFET: EMB20N03V

   Rds(ON)= 23 mohm (Vgs=5 V)
   I cont = 6 A (T =25)
   I peak = 32 A

   L-side MOSFET: EMB20N03V

   Rds(ON)= 23 mohm (Vgs=5 V)
   I cont = 6 A (T =25)
   I peak = 32 A

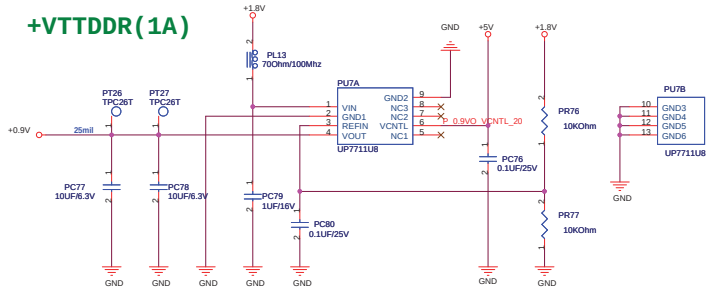
Controller

1. Voltage & Current:
   +1.8V@5.725A
2. Frequency:
   PR65=820K ohm
   Fosc=300KHz
3. OCP:
   PR66=15K ohm -> 13A
4. POR:
   Vccrth =3.7~4.1V
   Vcchys=0.2V
5. UVP:
   Vout*70%
6. OVP:
   Vout*115%
7. Enable Voltage:
   V = 2.9V
8. Soft start time:
   Tss=1.2 ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.15 A

0.9V@1.25A

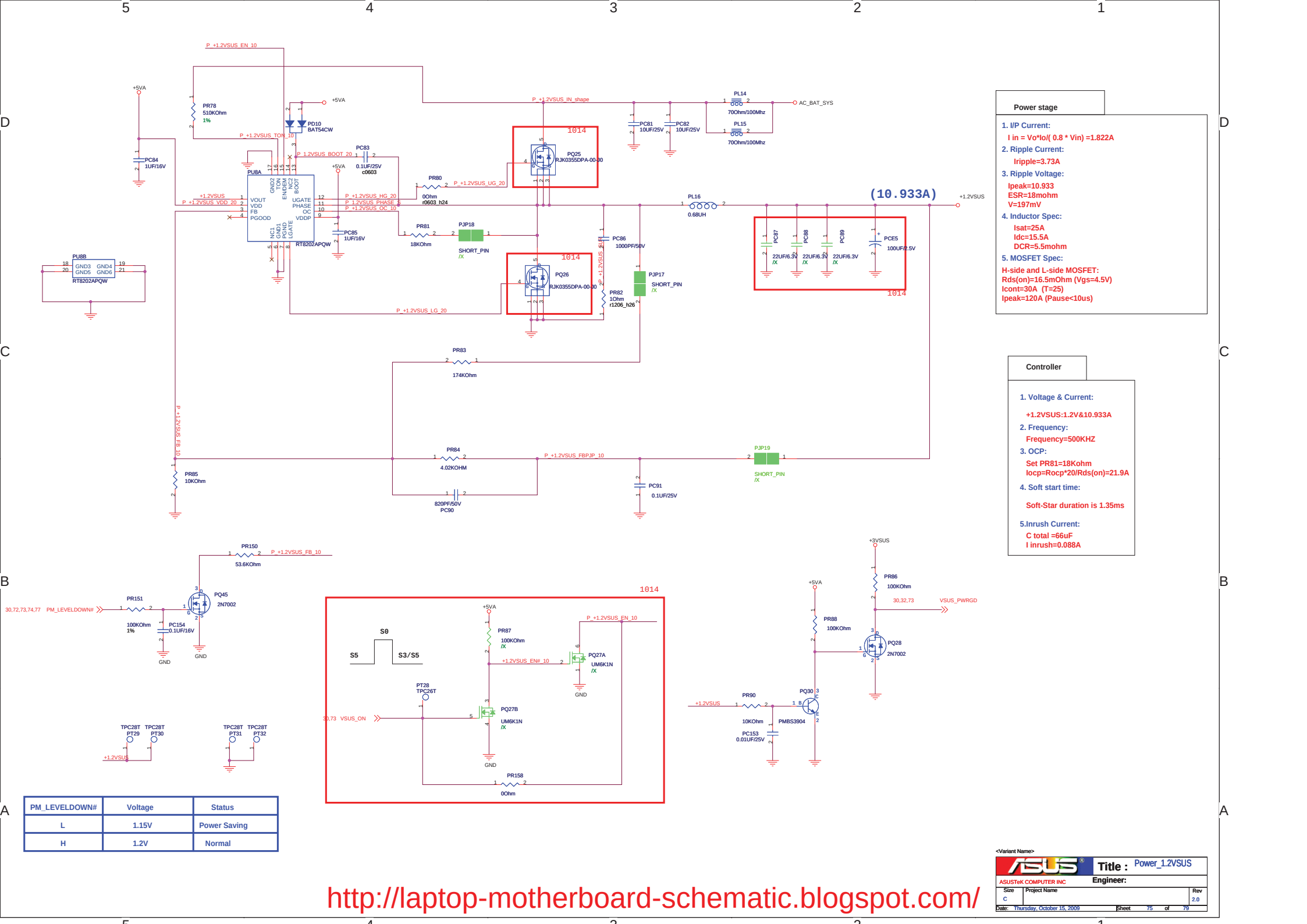
1. Dropout Voltage:
   〉V = 0.3V (Io = 2 A)
2. Current Limit:
   I limit = 4 A
3. Continue Current:
   I cont = 3 A
4. Power Dissipation:
   Rthjc = 52 /W
   Pd = 1.9 W
5. EN Voltage:
   V en = 1.4V
   V sd = 0.8 V
6. Supply Voltage:
   Vcc = 5 V
7. Inrush current:
   T ss = 5 ms
   C total = 10 uF
   I inrush = 3 mA

+VTTDDR(1A)



<Variant Name>

ASUSTek Computer INC	Title : +1.8V&VTTDDR	
	Engineer: N/A	
Size: A2	Project Name: 1201T	Rev: 2.0
Date: Thursday, October 15, 2009	Sheet 74 of 79	



Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.822A
2. Ripple Current:
   Iripple=3.73A
3. Ripple Voltage:
   Ipeak=10.933
   ESR=18mohm
   V=197mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:

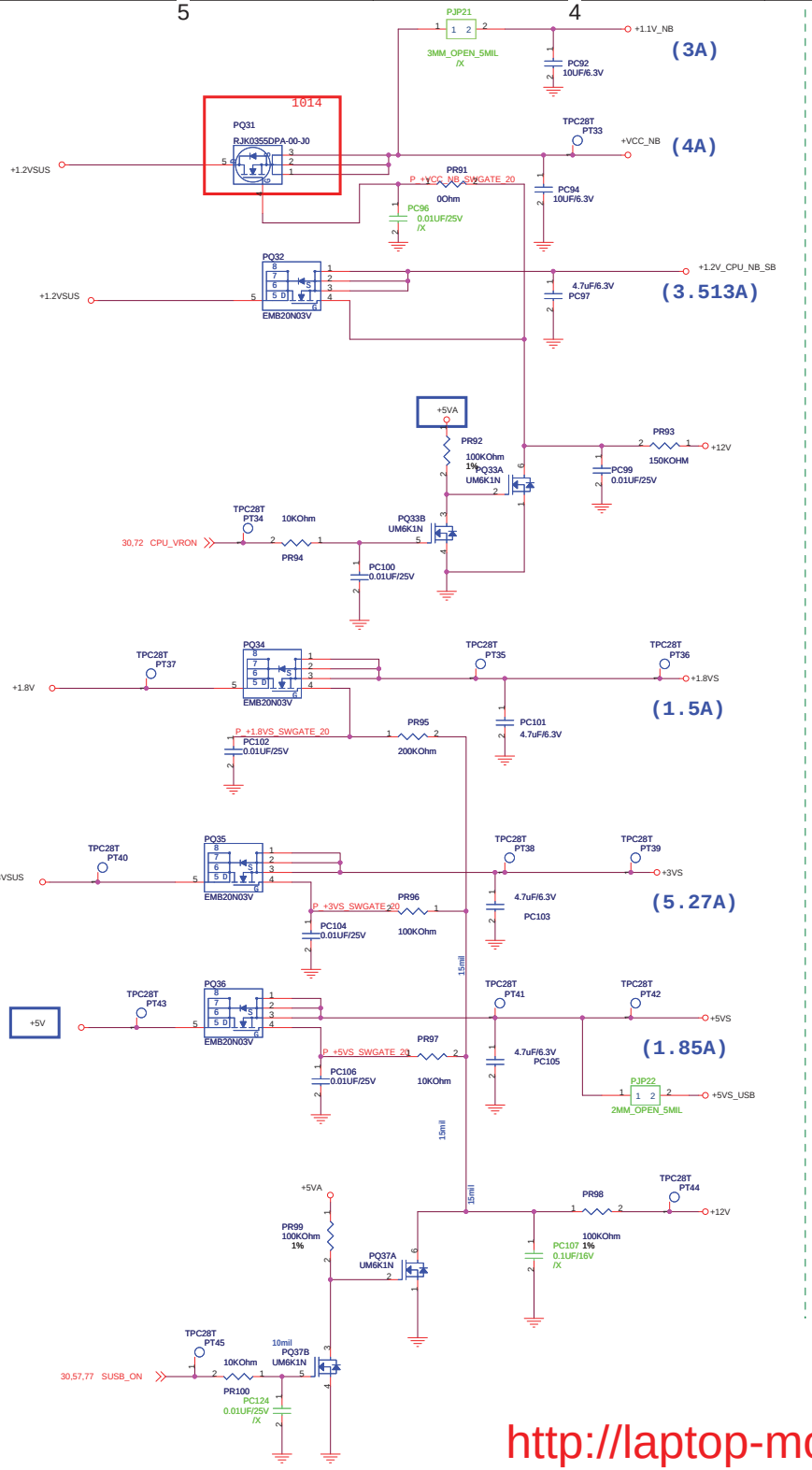
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

Controller

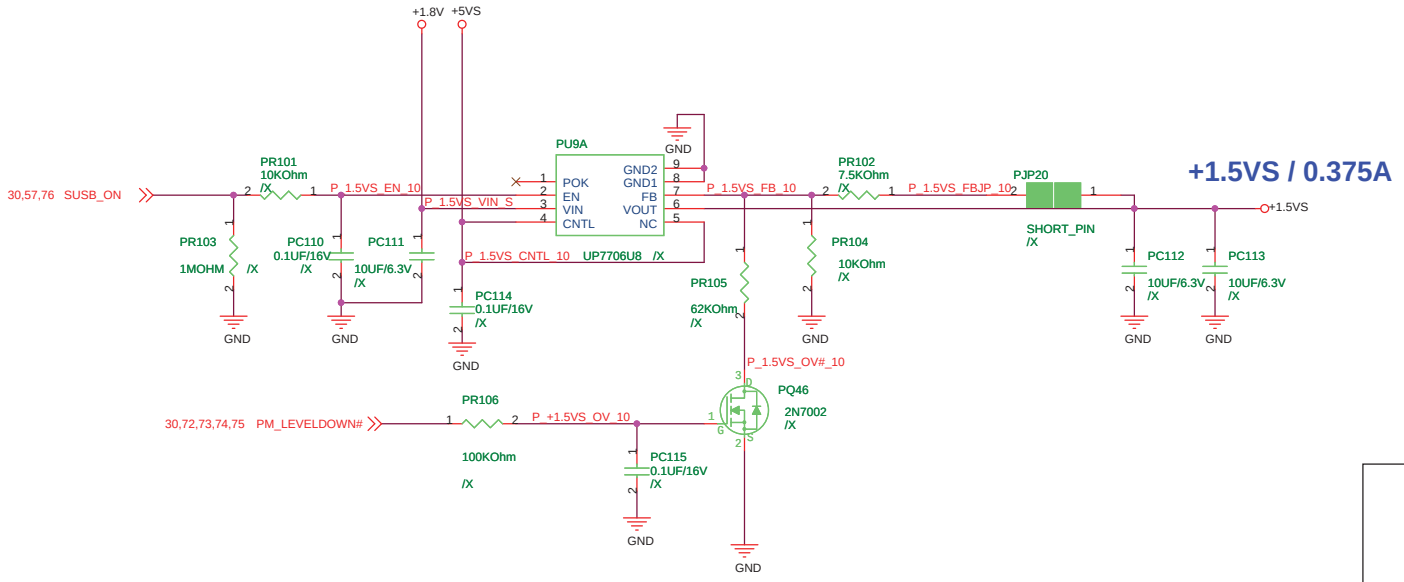
1. Voltage & Current:
   +1.2VSUS:1.2V&10.933A
2. Frequency:
   Frequency=500KHZ
3. OCP:
   Set PR81=18Kohm
   Iocp=Rocp*20/Rds(on)=21.9A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =66uF
   I inrush=0.088A

PM_LEVELDOWN#	Voltage	Status
L	1.15V	Power Saving
H	1.2V	Normal

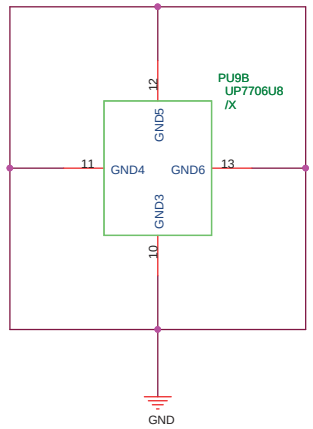
<Variant Name>
ASUSTeK COMPUTER INC
Title : Power_1.2VSUS
Engineer:
Size: C | Project Name | Rev: 2.0
Date: Thursday, October 15, 2009 | Sheet 75 of 79



<Variant Name>	Power_LOAD SWITCH OTHER
ASUSTeK COMPUTER INC	Title :
	Engineer:
Size: C	Project Name: 1201T
	Rev: 2.0
Date: Thursday, October 15, 2009	Sheet 76 of 79



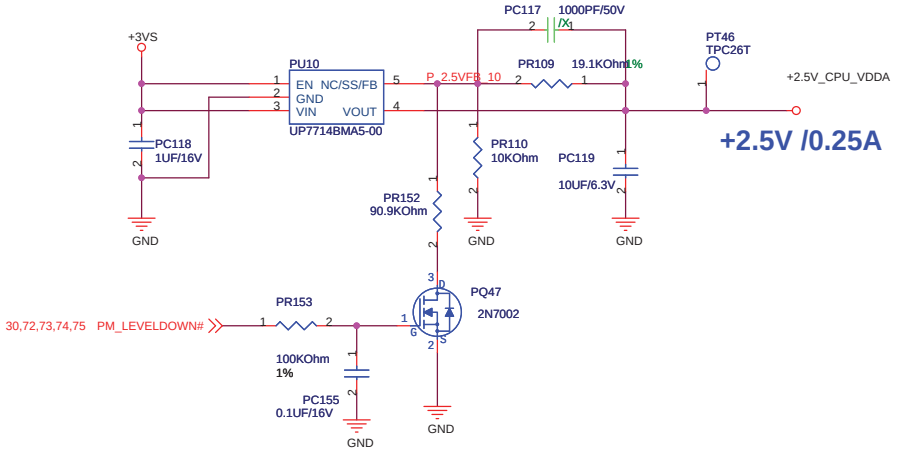
+1.5VS / 0.375A



PM_LEVELDOWN#	Voltage	Status
L	1.4V	Power Saving
H	1.5V	Normal

1. Dropout Voltage:
   〉 V= 300 mV (Io=2 A)
2. Current Limit:
   I limit= 2.8 A
3. Continue Current:
   I cont= 1A
4. Pd:
   R thjc =5 C/W
   Pd =1.9W
5. EN Voltage:
   V rising = 1.4 V
   V falling = 0.4 V
6. Supply Voltage:
   Vcc=5V
7. Inrush current:
   Tss = 4 ms
   C total = 20 uF
   I inrush= 7.5mA

PM_LEVELDOWN#	Voltage	Status
L	2.35V	Power Saving
H	2.5V	Normal



+2.5V /0.25A

2.5V @ 0.25A

1. Dropout Voltage:
   〉 V = 0.21V (Io =0.3A)
2. Current Limit:
   I limit =320mA
3. Continue Current:
   I cont = 300mA
4. Power Dissipation:
   Rthjc = 250 /W
   Pd = 0.4W
5. EN Voltage:
   V rising = 2V
   V falling = 0.8V
6. Supply Voltage:
   Vcc =3V
7. Inrush current:
   T ss = 400us
   C total =10uF
   I inrush = 0.063A

<Variant Name>

ASUSTek Computer INC

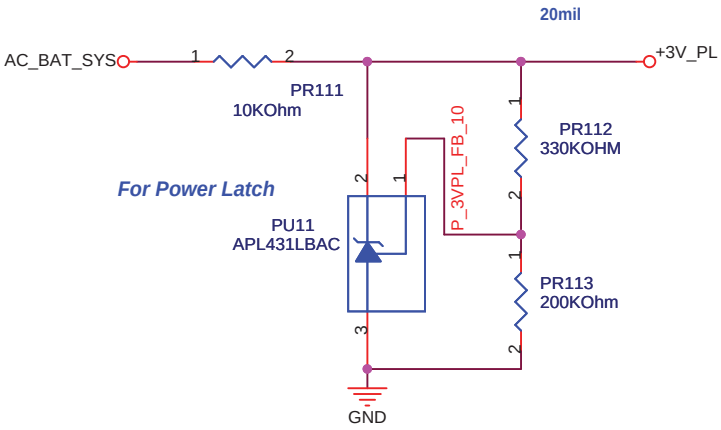
Title : +1.5VS & +2.5VS

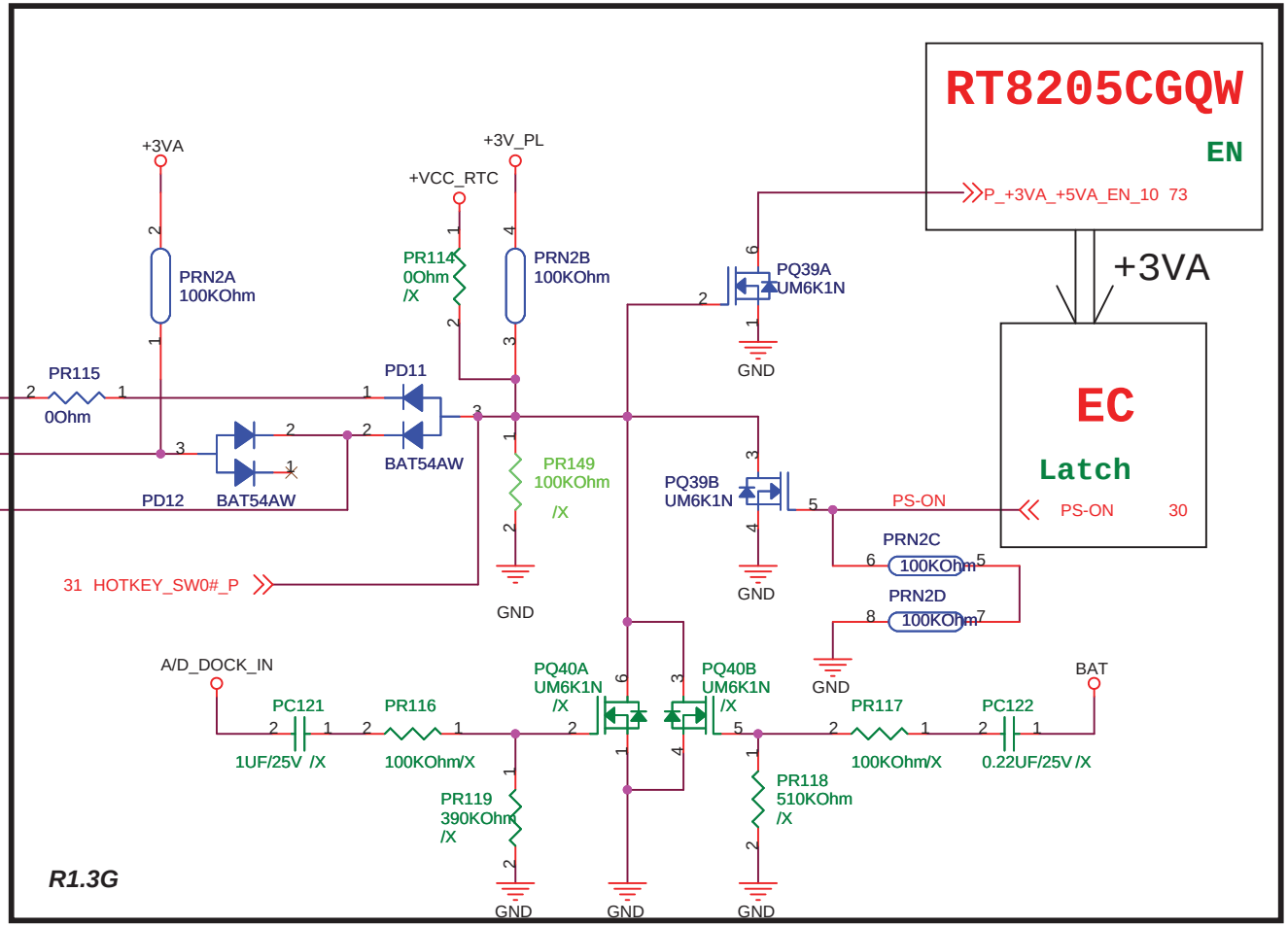
Engineer: N/A

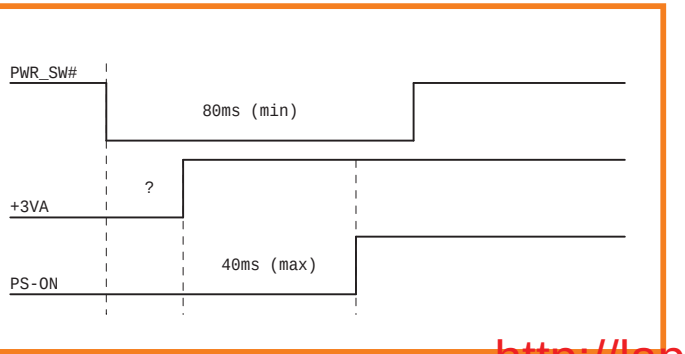
Size	Project Name	Rev
A3	1201T	2.0

Date: Thursday, October 15, 2009 Sheet 77 of 79

+3V_P L

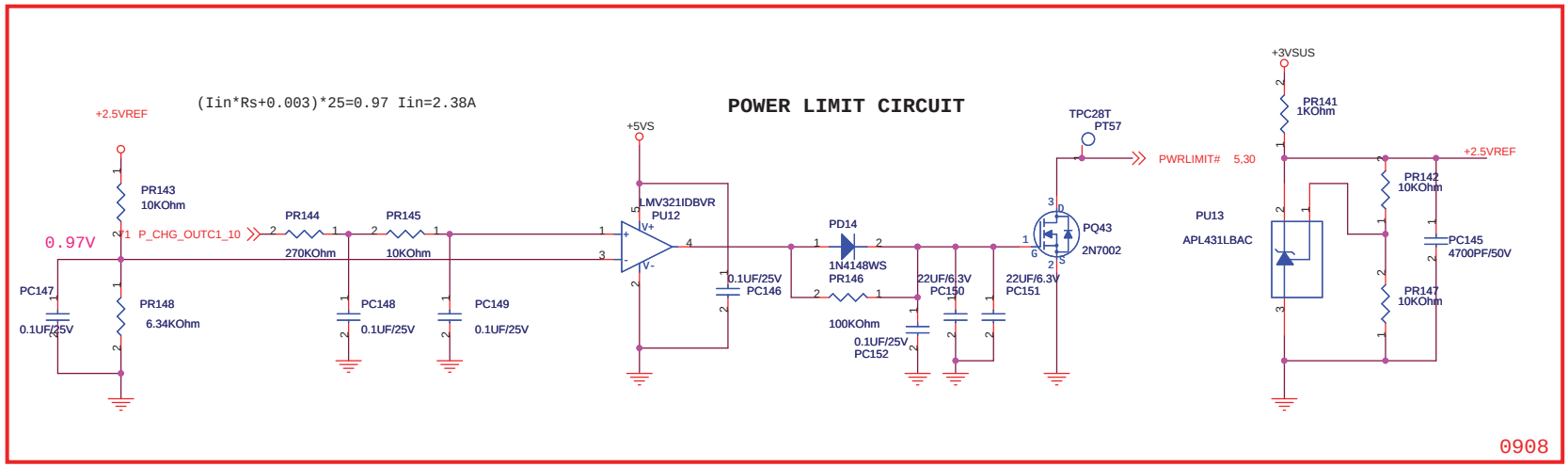






<Variant Name>

ASUSTek Computer INC.	Title : Power Latch	
	Engineer: N/A	
Size: A4	Project Name: 1201T	Rev: 2.0
Date: Thursday, October 15, 2009	Sheet 78 of 79	



<Variant Name>

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: N/A	
Size: A3	Project Name: 1201T	Rev: 2.0
Date: Thursday, October 15, 2009	Sheet 79 of 79	